Fortschritt-Berichte VDI

VDI

Reihe 10

Informatik/
Kommunikation

Yuhong Song, M. Sc.,
Yichang / China

Nr. 850

Suppressing Electromagnetic Interference in Switching Converters by Chaotic Duty Modulation

FernUniversität in Hagen
Schriften zur Informations- und Kommunikationstechnik

Suppressing Electromagnetic Interference in Switching Converters by Chaotic Duty Modulation

DISSERTATION

zur Erlangung des akademischen Grades

DOKTOR-INGENIEURIN

der Fakultät für Mathematik und Informatik

der FernUniversität in Hagen

von

Yuhong Song, M.Sc.

Yichang/China

Hagen, 2016

Fortschritt-Berichte VDI

Reihe 10

Informatik/
Kommunikation

Yuhong Song, M. Sc.,
Yichang / China

Nr. 850

Suppressing Electromagnetic Interference in Switching Converters by Chaotic Duty Modulation

FernUniversität in Hagen
Schriften zur Informations- und Kommunikationstechnik

Song, Yuhong
Suppressing Electromagnetic Interference in Switching Converters by Chaotic Duty Modulation
Fortschr.-Ber. VDI Reihe 10 Nr. 850. Düsseldorf: VDI Verlag 2017.
104 Seiten, 64 Bilder, 18 Tabellen.
ISBN 978-3-18-385010-5, ISSN 0178-9627,
€ 43,00/VDI-Mitgliederpreis € 38,70.

Keywords: Switching power supply – Switching converter – Chaotic duty modulation – Electromagnetic interference (EMI) – Electromagnetic compatibility (EMC) – Stability – Remaining useful life

Abstract: The switching converter generates serious electromagnetic interference (EMI), which impairs other devices' performance and harms human being's health. As a way of chaos technique, chaotic modulation has been developed to suppress EMI of the switching converter by dispersing the energy into a wide frequency band and smoothing the peaks of the EMI spectrum. Unlike the well-studied chaotic frequency modulation, the chaotic duty modulation is concerned in this dissertation, which is just to change the duty of the transistor driving-pulse while maintains the fixed switching frequency. Chaotic duty modulation is realized by appending an external chaotic signal to the existing PWM module of the switching converter, which is practicable without the loss of the generality. It is thus verified that this proposal of using chaotic duty modulation in switching converters for EMI suppression is feasible and lays a foundation for industrial applications.

Bibliographische Information der Deutschen Bibliothek
Die Deutsche Bibliothek verzeichnet diese Publikation in der Deutschen Nationalbibliographie; detaillierte bibliographische Daten sind im Internet unter http://dnb.ddb.de abrufbar.

Bibliographic information published by the Deutsche Bibliothek
(German National Library)
The Deutsche Bibliothek lists this publication in the Deutsche Nationalbibliographie (German National Bibliography); detailed bibliographic data is available via Internet at http://dnb.ddb.de.

Schriften zur Informations- und Kommunikationstechnik
Herausgeber:
Wolfgang A. Halang, Lehrstuhl für Informationstechnik
Herwig Unger, Lehrstuhl für Kommunikationstechnik
FernUniversität in Hagen

Als Manuskript gedruckt. Printed in Germany.
ISSN 0178-9627
ISBN 978-3-18-385010-5

Acknowledgements

My former colleague at the Shunde Polytechnic, Dr. Ping Li, introduced me to Prof. Wolfgang A. Halang in 2010 as he visited our laboratory. Wonderfully, the casual meeting has greatly changed my life, just like "butterfly effect" in the chaos theory, which has been used in my research work for my Ph.D degree. In the following year, I was invited to work for a project funded by German Industry Association, meanwhile, to pursue my Ph.D degree at the FernUniversität in Hagen.

Before 2010, I only knew that "butterfly effect" relates to one sentence, "A butterfly from the Amazon river basin rainforest in South America, occasionally flaps its wings, which could cause a tornado in Texas of the United States two weeks later". With the further study, I understood the real meaning behind "butterfly effect", which is the poetic description of the chaotic phenomenon. Together with relativity and quantum mechanics, chaos is considered as one of the three monumental scientific discoveries in the twentieth century. Our real world is essentially nonlinear, thus chaos is ubiquitous, attracting so much research interest in the past few decades. However, for a long time, chaos has been considered to be harmful and useless, and thus controlled to prevent its appearance in the nonlinear systems. Recently, chaos has been found helpful and useful for some engineering applications, such as secure communication, motor control and electromagnetic interference (EMI) suppression. However, the research achievements are mostly embodied in the theory and laboratory prototype and industrial applications have been in a wait-and-see status.

The idea of trying to offer the feasible schemes for commercial switching converters motivated me to make a research on applying chaos in reducing EMI. Chaos technique has been applied in switching converters in two ways: parameter control and spread spectrum modulation. The parameter control is strictly demanded to maintain chaos under various conditions, i.e., different loads, which results in the complexity of system design. Chaotic modulation has been developed to suppress EMI of switching converters by dispersing the energy into a wide frequency band and smoothing the peaks of the EMI spectrum. My research, focusing on chaotic duty modulation, has proposed the spread spectrum schemes in commercial switching converters. Meanwhile, simulations and experiments have been conducted to verify the effectiveness of the proposed schemes on EMI reduction. Furthermore, on the basis of spectral properties of chaotic signal, which is normally represented by Fourier Transform, the central frequency has been defined to be the frequency corresponding to the greatest spectral peak of chaotic signal. It has been proved that the chaotic duty modulation is the most effective to suppress EMI when the central frequency of chaotic signal is equal to the switching frequency of transistor in switching converters.

This thesis bears painstaking efforts of many persons. First of all, I would like to express my sincere gratitude to my supervisor Prof. Zhong Li for his guidance with patience. Without his keen insight and constant encouragement, my thesis would not have appeared in the present form. I would also thank his wife, Mrs. Juan Mei, for her concern to my

daily life. Further, I would like to thank my co-advisor Prof. Wolfgang A. Halang for his continuous support and kindly help in both my work and daily life, and thank his wife, Mrs. Halang, for her kindness.
Special thanks go to my colleagues Mrs. Junying Niu and Dr. Guidong Zhang for their great co-operation, fruitful discussion, encouragement and care through the whole course of my Ph.D study. I would also thank Mrs. Jutta During and Mr. Schubert for their technical support at the FernUniversität in Hagen, Germany. I am very grateful to Prof. Holger Hirsch for his support to carry out my experiment at University of Duisburg-Essen, Germany. My appreciation goes to Dr. Wenping Xiao, Dr. Yajun Li and Dr. Fan Xie for giving me a lot of suggestions about my thesis. I owe my thanks to Dr. Ping Li for her recommendation and also thank my German friends Mr. and Mrs. Dannert, Mr. and Mrs. Fisher for their kindness.
Cordial thanks also go to my family for the love and concern all the time, to my parents and mother-in-law for their consideration, to my husband for his understanding and support, and to my son, who is a sunny boy and encourages me to engage in the scientific research. In addition, my greatest gratitude goes to my sister Dr. Yinhong Song for her encouragement and help.
Sincere thanks go to the Shunde Polytechnic, whose policy of training personnel benefits my scientific research and Ph.D study in Germany.

Contents

Abstract

A switching power supply, namely switching converter, which is characterized by high efficiency, small volume and light weight, has developed rapidly in recent years and has been gradually deployed instead of linear power supplies in electronic and electrical domains. The switching power supply makes use of the pulse-width modulation (PWM) technology to control the nonlinear components, so that they have a switching action of high frequency, resulting in high change rates of voltage and current. Consequently, the switching converter generates serious electromagnetic interference (EMI), which impairs other devices' performance and harms human being's health. Hence, suppressing EMI has become a common concern in the design and the application of switching converters.

Traditionally, EMI is dealt by filtering or shielding, or both. Filtering aims to reduce the conducted EMI by adding the filters to the system. In practice, multiple filters should be employed in a switching converter because a single filter is restricted by its narrow frequency band. Shielding aims to block the converter from emitting or receiving the radiated EMI with barriers made of conductive material. These traditional filtering and shielding techniques have the disadvantages in weight, size and cost, and their engineering applications depend on the experience of engineers. Additionally, it has been found that soft switching technique can be used to reduce EMI. However, it needs an auxiliary control module to guarantee zero voltage or zero current during the transformational period of transistors, resulting in a complicated design. Hence, using chaos in switching converters has become new preferable technique to tackle the EMI problems due to the pseudo-random and continuous spectrum characteristics of chaos.

As a way of chaos technique, chaotic modulation has been developed to suppress EMI of the switching converter by dispersing the energy into a wide frequency band and smoothing the peaks of the EMI spectrum. It is well known that the effectiveness of EMI suppression is related to chaotic signals used for chaotic modulation. From this study, it is further found that the central frequency of a chaotic signal, corresponding to the largest peak of its frequency spectrum, should be close to a half of the switching frequency of a power supply to reach optimal EMI suppression.

Unlike the well-studied chaotic frequency modulation, the chaotic duty modulation is concerned in this dissertation, which is just to change the duty of the transistor driving-pulse while maintains the fixed switching frequency. Chaotic duty modulation is realized by appending an external chaotic signal to the existing PWM module of the switching converter, which is practicable without the loss of the generality.

It is followed with a qualitative verification of the stability of power supplies under chaotic duty modulation via the classic control theory, and practically, the useful life through the failure model and critical components, which is also ensured under chaotic duty modulation. It is thus verified that this proposal of using chaotic duty modulation in switching converters for EMI suppression is feasible and lays a foundation for industrial applications.

Key Words: Switching power supply, Switching converter, Chaotic duty modulation, Electromagnetic interference (EMI), Electromagnetic compatibility (EMC), Stability, Remaining useful life

1 Introduction

1.1 Switching Converters

A power supply is the device which transforms the electrical energy between the alternative current (AC) and the direct current (DC), or changes the voltage or frequency [1]. It makes use of the rectifier or the inverter, or both. A rectifier converts AC into DC while an inverter DC into AC, which are called AC-DC converter and DC-AC converter respectively. The cascade of the inverter and the rectifier changes the amplitude of DC output, which is named DC-DC converter. Having the rectifier and the inverter connected in series will change the frequency or amplitude of AC, which is AC-AC converter. One switching mode power supply, namely a switching converter, completes the transformation of the electrical energy in a circuit by controlling switching actions of transistors to obtain a stable output. Hence, the technology of switching converters involves the circuit topology, transistor and switching control approach.

There are many converter topologies [2] categorized according to how many transistors are used and whether a transformer is employed to isolate the output from the input electrically. Buck and boost converters are the basic non-isolated single-transistor topologies, based on which other non-isolated converters have been developed, such as buck-boost, Cuk, Zeta and single ended primary inductor converters. The isolation topologies include the single-transistor forward and backward converters, two-transistor half-bridge and four-transistor full-bridge converters. All the single-transistor converters are normally applied in small-medium power outputs while the multiple-transistor ones are widely used in medium-large power outputs. Each topology has its pros and cons.

Power semiconductor technology labels the development of power electronics [3]. Bell Labs developed the first p-n-p-n silicon controlled rectifier (SCR) in 1957, which opened the new era of power electronics. Afterwards, bipolar junction transistors (BJT), metal-oxide-semiconductor field-effect transistor (MOSFET) and insulated gate bipolar transistor (IGBT) appeared. Up to now, power semiconductor devices have been improved and innovated for the characteristics of high current, high voltage, low conducting loss and high switching frequency.

The converters adopt the principle of pulse modulation to control the switching actions. According to the output feedback, the frequency or width of the transistor driving-pulses is modulated to obtain stable outputs. Between the two ways, pulse-width modulation (PWM) is mostly applied in switching converters. A PWM module is composed of discrete components or an integrated circuit (IC) with several peripheral elements. Nowadays, the module normally uses the customized PWM ICs, such as TL494, SG3525 and UC3842.

Along with the development of IC and power semiconductor technology, switching converters have been characterised by small size, high working frequency and high efficiency [4]. Because of applying some nonlinear components such as the transistor, transformer and

diode, and deploying the PWM technology to control switching actions of the transistor, the converter produces high change rates of current and voltage, resulting in the serious electromagnetic interference (EMI). Therefore, the switching converter has become an emission source of EMI to its surroundings, which hinders the development and the application of switching converters.

1.2 EMI and EMC

1.2.1 EMI Elements

EMI refers to any electromagnetic phenomenon possibly either doing harm to the life and the nonliving, or causing device, equipment and system degrading performance [5]. As shown in Figure 1.1 [6], EMI includes three elements, namely, disturbing source, coupling channel and receiver. Through conducting or radiating, a device or system emits EMI to its environment. The radiated disturbance, especially with the frequency range from 30 MHz to 1 GHz, spreads itself via the space with the characteristics of electromagnetic wave. The conducted disturbance, with the frequency range from 150 kHz to 30 MHz, transmits itself via the conductor connected physically between the source and the receiver. It is the immunity that keeps device, equipment or system from degrading their performance under the EMI. Electromagnetic compatibility (EMC) is defined as the ability of an equipment to function satisfactorily in its electromagnetic environment without introducing intolerable electromagnetic disturbance to other equipments in the same environment. Hence, on one hand, some measurements should be taken to suppress EMI resulting from high change rates of current and voltage in switching converters. On the other hand, the converters should have the immunity to the electromagnetic disturbance from its surrounding and other equipments or devices.

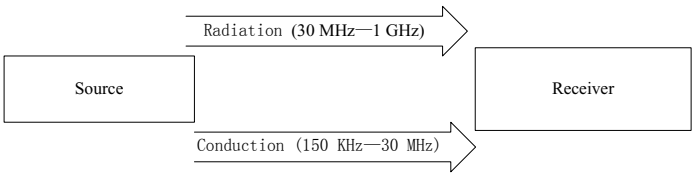


Figure 1.1: Three elements of EMI

1.2.2 EMC Test

Facing the unwanted EMI, the international communities have agreed on standard regulations, i.e. the EMC standards, which are supposed to ensure all kinds of electronic

and electrical equipments to comply with regulatory requirements. The relevant basic standards called up in EN61204-3 are: EN55022 and EN55011.
As above mentioned, switching converters emit the conducted and/or radiated EMI, in which the conducted EMI dominates because of the operation frequency range of converters. Therefore, the EMI refers to conducted disturbance here and throughout the dissertation. An receiver is normally applied to test conducted EMI, which involves three options: peak (PK), quasi-peak (QP) and average (AV), respectively. The EMI test, as the major part of EMC test for switching converters, is categorized into Class A applied in industry and Class B applied in home application, in which the latter is more stringent. Take the PC's power supply as an example. The conducted disturbance test is implemented according to EN55022 Class B conducted QP and EN55022 Class B conducted AV. The frequency range and the limits are demonstrated in Figure 1.2. The red line presents the emission limit under Class B conducted QP test, and the blue presents the emission limit under Class B conducted AV test. The test is passed when the testing curve is under the corresponding limit, otherwise it is unqualified. The testing curves demonstrated in Figure 1.2 indicate that the equipment has passed the test.

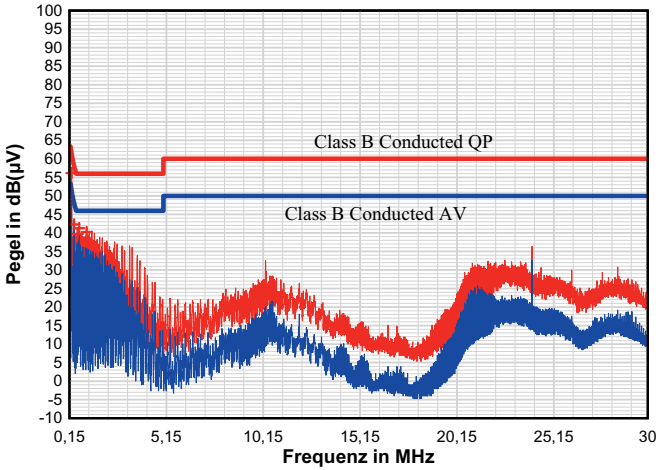


Figure 1.2: Conducted EMI test under EN55022 Class B

1.2.3 Visualization of EMI

A time domain signal, i.e. the transistor driving-pulse in a switching converter, can be observed by transforming to a frequency domain signal with Fourier Transform [7]. The

main idea of Fourier Transform is that any periodical signal can be transformed to a discrete spectrum and any aperiodic signal can be transformed to a continuous spectrum. Denote $f(t)$ as a time domain signal. If it is periodical, its Fourier series in exponential form is expressed by

$$f(t) = \sum_{n=-\infty}^{\infty} F_n e^{jn\omega t}, \tag{1.1}$$

where F_n is the n-th series coefficient, and ω is the angular frequency. Denote t_0 as the initial instant of the cycle and T the width of the cycle. F_n is given by

$$F_n = \frac{1}{T} \int_{t_0}^{t_0+T} f(t) e^{-jn\omega t} dt. \tag{1.2}$$

F_n presents the amplitude at the corresponding frequency of $f(t)$ in frequency domain, and it is named as the spectral component or the spectral coefficient.
If $f(t)$ is aperiodic, its Fourier Transform leads to a continuous spectrum. $f(t)$ can be expressed as

$$f(t) = \frac{1}{2\pi} \int_{-\infty}^{\infty} F(\omega) e^{j\omega t} d\omega. \tag{1.3}$$

$F(\omega)$ is the spectrum density function and defined as

$$F(\omega) = \int_{-\infty}^{\infty} f(t) e^{-j\omega t} dt. \tag{1.4}$$

According to the Parseval theory [8], the energy spectrum density of $f(t)$ can be calculated. If $f(t)$ is periodical, its energy spectrum density is

$$S_n = |F_n|^2. \tag{1.5}$$

If $f(t)$ is aperiodic, its energy spectrum density is

$$S(\omega) = |F(\omega)|^2. \tag{1.6}$$

Figure 1.3 demonstrates the periodical transistor driving-pulse and its spectrum in a DC-DC converter operating at the frequency of 30 kHz. All peaks scatter at the fundamental component of the switching frequency and harmonics. Each peak value reflects the energy of the corresponding frequency. In Figure 1.3, F_1, F_2, F_4 and F_7 are the fundamental component, 2nd, 4th and 7th harmonic component, respectively.
Figure 1.4 shows the current through the output inductor and its spectrum when the converter operats at the frequency of 50 kHz. The spectrum is continuous due to the aperiodic current, but it can be observed that there are some peaks at the fundamental

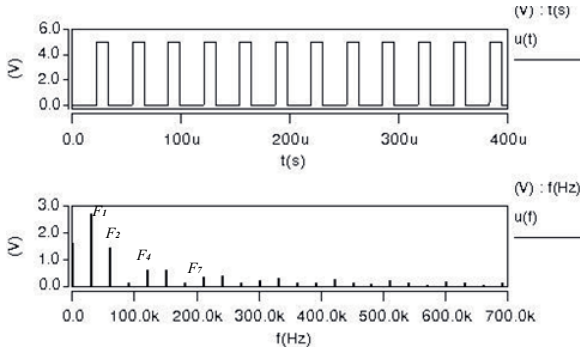


Figure 1.3: Periodic signal (upper) and its FFT (lower)

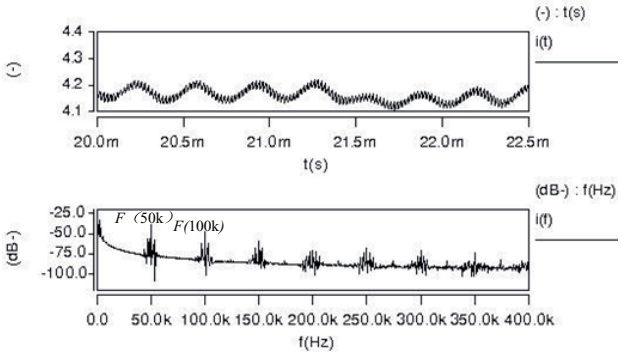


Figure 1.4: Aperiodic signal (upper) and its FFT (lower)

component and harmonics. As shown in Figure 1.4, $F(50\ \mathrm{k})$ and $F\ (100\ \mathrm{k})$ are the fundamental component and 2nd harmonic respectively.
In summary, for periodic and aperiodic signals, their EMI can be observed and measured by their frequency spectra with Fourier Transform. The signal energy can be estimated according to the spectral amplitudes of the fundamental component and harmonics, which is the basic of mathematical analysis and experimental test for EMI.

1.3 EMI Suppression in Switching Converters

1.3.1 Filtering and Shielding

EMI reduction techniques have been developed and applied by considering the above mentioned three elements: disturbing source, coupling channel and receiver.
Some measures are taken to suppress EMI by fighting the disturbing source, which weaken the EMI generation or reduce the EMI emission. Normally, the heat sink of switching converter is tightly grounded to avoid changing the electrical potential, which facilitates to weaken the EMI generation. Then, the active shielding is often amounted to reduce the EMI emission. Additionally, the optimization of hardware design is also effective to weaken the EMI generation and reduce the EMI emission, which involves the printed circuit board (PCB) wiring, the component layout, transformer winding and so on.
EMI filtering is normally used to cut off the coupling channel to suppress EMI from the aspect of transmitting the disturbance. As seen in Figure 1.5, the filters, which use the choking inductors ($L_1L_2L_3$ and L_4) and the filtering capacitors (C_1C_2 and C_3), are physically connected to the coupling channel of the conducted interference and blocks the interference passing between the public grid and the main circuit.

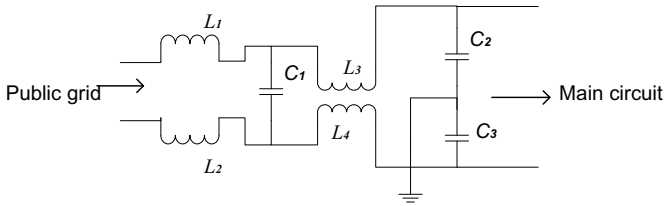


Figure 1.5: EMI filter

To suppress EMI from the aspect of receiver or victim, the passive shielding is mainly used to avoid receiving the external disturbance.
However, the above methods have their own drawbacks. Because transistors, inductors and capacitors possess the distribution properties of component characteristics, the effectiveness of optimized designs and their applications depend on the experience of designers and

engineers, increasing the complexity of system design. Multiple filters should be applied to execute filtering in a wide frequency range, because a single filter works just for a narrow frequency band, which increase the hardware cost and volume. In recent decades, the researchers have been focusing on the mechanism of the interference sources and proposed soft switching techniques and chaos techniques.

1.3.2 Soft Switching

The voltage and current change sharply when transistors turn on or shut off under the normal PWM control, which is called the hard switching. Because neither of the voltage and current equals zero during the switching period, the instantaneous power of transistors ($p(t) = u(t)i(t)$) exists during the process of switching from "ON" to "OFF" and vice versa, which results in the switching loss and noise. Consequently, the higher the working frequency of transistors is, the heavier the switching loss and noise will be.

The Soft switching technique was first presented [9] in 1990 and has rapidly developed in recent years, which makes up for the deficiency of the hard switching. Many researchers have proposed a variety of soft switching techniques, such as the resonant or the quasi-resonant converter [10], zero current switching PWM converter [11, 12], and zero voltage switching PWM converter [13–15] since 1993. Using soft switching technique, transistors are turned on with zero current and turned off with zero voltage through importing resonance. As shown in Figure 1.6, the transistor Q is turned off at t_0 , and the switching current $i_Q(t)$ falls to zero until t_1. At the same time, the voltage across the transistor Q rises from zero in sinusoidal way. Therefore, the instantaneous power $p(t) = u_Q(t)i_Q(t)$ becomes tiny while turning off. In the same way, the current through the transistor Q rises from zero in sinusoidal way and the instantaneous power is also tiny while turning on, which reduces the switching loss and noise. Meanwhile, the high change rates of voltage and current of transistor are alleviated, thus the EMI can be reduced.

However, one auxiliary switch circuit is demanded in the soft switching system, which gives rise to increasing the difficulty of control. The improper control will increase EMI, so it is not sure that the soft switching techniques can improve EMC of switching converters.

1.3.3 Chaos Technique

Mathematically, chaos means a deterministic aperiodic behavior, which is characterized by the pseudo-random and continuous spectrum. The switching converter will exhibit chaotic behaviours under chaos, so that the spectral fundamentals of the switching voltage and current and their harmonics scatter their energies to an extended bandwidth, which implies the EMI suppression. Therefore, chaos technique attracts the attention and interest of the researchers in EMI reduction of switching converters. Chaos technique is applied in switching converters by two methods: parameter control [16–19] and spread spectrum modulation [20–23].

a. Parameter Control

This method refers to making the system chaotic through adjusting some parameters, such as the feedback coefficient [18] and the reference of current and voltage [17]. The controlled

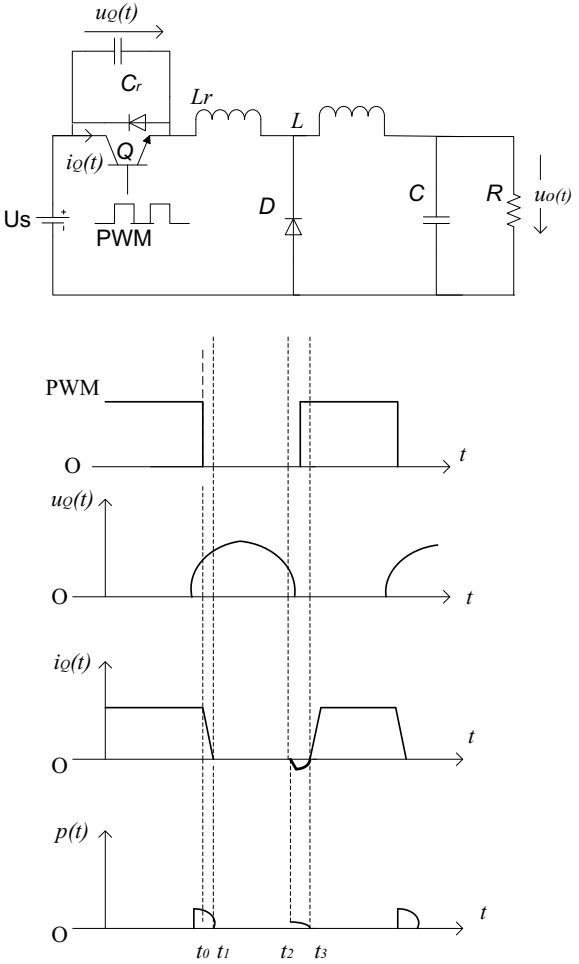


Figure 1.6: Soft switching circuit and working waves

parameter should be precisely adjusted to maintain chaos under various conditions, i.e., different loads, which makes it difficult to design the system and implement the hardware.

b. Spread Spectrum Modulation

Basically, spread spectrum modulation is realized by attaching an external disturbance to PWM control module, which modulates the duty or frequency of transistor driving-pulses [17, 21, 22, 24–29]. Thus, the energy is expanded to a wide bandwidth and the EMI peaks are flattened. It is demonstrated in Figure 1.7 that the peak at f_O is modulated to $[f_O - \Delta f, f_O + \Delta f]$ and the amplitude is reduced. Spread spectrum modulation is depicted by modulation mode and modulation signal.

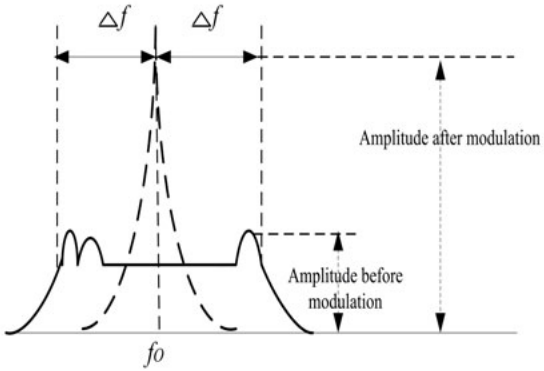


Figure 1.7: Spread spectrum modulation

Four modulation modes have been reported [30–32]: pulse width modulation with varying duty and fixed cycle (PWM), pulse position modulation with varying position of pulse and fixed cycle (PPM), frequency modulation with varying duty (FMVD) and with fixed duty (FMFD). By analyzing the power spectrum density of output signals, it has been proved that all the above modulations can reduce the amplitudes of spectral fundamental component of switching frequency and harmonics [24].

Both periodic and aperiodic signals can act as the modulation signals, among which aperiodic ones mainly refer to random signals and chaotic signals. The effectiveness of spread spectrum varies among different modulation signals under the same modulation mode [29]. Denote f_S as the switching frequency under normal PWM control. The frequency modulation with fixed duty is taken as an example of modulation mode, under which three kinds of modulation signals have been used: periodic signal, random signal and chaotic signal.

The periodic signal has a fixed frequency denoted by f_P and its spectrum is intermittent. Periodic modulation makes the energies at harmonics of switching frequency $nf_S(\mathrm{n}\in \mathrm{Z}, and\ \mathrm{n}\geq 1)$ spread over the frequency band with an interval of $f_P$which reduces the amplitudes at harmonics nf_S [29].

The random signal has a continuous and smooth spectrum. Random modulation makes the energies at harmonics of switching frequency $nf_S(\mathrm{n}\in \mathrm{Z}, and\ \mathrm{n}\geq 1)$ spread over the frequency band averagely, which flattens the peaks [29].
The chaotic signal is of pseudo-randomness with a continuous spectrum, but it is not smooth. Chaotic modulation makes the energies at harmonics of switching frequency $nf_S(\mathrm{n}\in \mathrm{Z}, and\ \mathrm{n}\geq 1)$ fluctuate over the whole spectral range [29].
Thus, period modulation distributes the energy in discrete points, which has the least effectiveness. Chaotic modulation spreads the energy into a wide frequency band with a continuous and fluctuant spectrum, which is less effective for spread spectrum. Random modulation spreads the energy over a continuous and smooth spectrum, which is the most effective for spread spectrum. However, it is difficult to obtain the genuine random signal and it is costly to manufacture the random generator [29]. Taken all together, chaotic signal is more suitable for commercial applications due to the less cost for generators and the better effect for spread spectrum modulation.
Factually, chaotic frequency modulation is the most common modulation reported about spread spectrum [21, 22, 29], where the frequency of transistor driving-pulse is modulated by a chaotic signal. However, this modulation possesses the varying frequency of transistor driving-pulse, which causes the difficulty in designing circuitry parameters.

1.3.4 Effect of Chaotic Signal on Modulation

Some researches [22, 33] have probed the characteristics of chaotic signal used by chaotic modulation. Based on statistical theory and random point process theory, the characteristic function and probability density function of PWM driving pulses under chaotic frequency modulation have been analyzed, by which the effectiveness of chaotic modulation to EMI suppression in converters has been theoretically verified [33]. Lorenz, Chua's circuit, Rossler third-order and forth-order circuits have been respectively used to generate a chaotic signal as the modulation signal [20]. It has been found that use of Lorenz signal is most effective for EMI reduction under chaotic frequency modulation. Another scheme of chaotic frequency modulation has been designed to suppress EMI in DC-DC boost converters by connecting an external Chua's chaotic signal to modulate the frequency and amplitude of the sawtooth [22], in which the frequency of Chua's oscillator needs to be close to the switching frequency in order to reach the best effectiveness of EMI reduction.
The spectral characteristics of chaotic signal have been concerned by the above researchers, which manifests itself as spectral distribution, i.e. spectral peaks and width. Although a small amount of literature is involved in studying the effect of chaotic signal on chaotic modulation, it is evident that the effectiveness of EMI suppression is related to the spectral characteristics of chaotic signal used by chaotic modulation.

1.4 Motivation

Chaotic modulation has a promising application for EMI suppression in switching converters due to the pseudo-random and continuous spectrum characteristics of chaos. Nowadays,

research achievements of chaotic modulation are mostly embodied in the theory and laboratory prototype, but its real industrial applications have not been witnessed. Chaotic frequency modulation has been the most commonly reported about EMI suppression in switching converters, which features the varying working frequency. Because the operations of nonlinear component, such as the transistors and transformers, are susceptible to the varying frequency, chaotic frequency modulation will increase the difficulty in designing circuitry parameters. Chaotic signals, as modulation signals, their spectral characteristics affect the effectiveness of EMI suppression, which still lacks a quantitative estimation. Thus, combined with the modulation mode and modulation signal, practical schemes of EMI reduction for commercial power supplies are needed. And, for a practical scheme, its system performance should comfort to the corresponding specifications such as EMC standards before launching it in the market.

Having this consideration in mind, we focus on chaotic duty modulation instead of chaotic frequency modulation. Chaotic duty modulation possesses the fixed frequency, which can not only overcome the disadvantages of chaotic frequency modulation, but also facilitate the operations of transistors and high frequency transformers. Chaotic modulation will be realized by connecting an external chaotic signal to the PWM integrated circuit (IC). In order to obtain the typical practical scheme without any loss of generality, a commercial power supply, i.e., a personal computer's (PC's) power, will be regarded as the objective based on two aspects. On one hand, it is of half-bridge topology, which represents the medium-power type widely used in commercial switching converters. On the other hand, it possesses a PWM module, a typical IC applicable to many topologies. Simulations and experiments will be carried out to further verify the effectiveness of the proposed scheme for EMI reduction.

Meanwhile, we will make an intensive study about the effect of chaotic signal on EMI suppression. In order to analyze the chaotic signal conveniently, its central frequency will be defined as the frequency of its largest spectral peak. With the help of the central frequency, it can be quantitatively estimated whether the spectral characteristics of chaotic signal is suitable for the chaotic modulation.

Additionally, we will apply the classic control theory for analysing the system stability under chaotic duty modulation and deduce two prerequisites for the chaotic signal. Then, effects of chaotic modulation on the remaining useful life will be investigated. Finally, for the scheme of PC's power supply, system input and output characteristics under chaotic modulation will be tested and compared with those under normal PWM control.

1.5 About the Dissertation

The dissertation is organized as following.

Chapter 1 reviews the main techniques of EMI suppression in switching converters, and in the meantime, introduces the background and significance of this research, and summarizes the contents as well as the innovations.

The following chapter proceeds chaotic duty modulation comparing with chaotic frequency modulation. Mathematical deductions and computer simulations are separately conducted

for these two modulation modes, which demonstrate that chaotic duty modulation is effective for EMI suppression in switching converters just like chaotic frequency modulation.
Chapter 3 defines the central frequency as the corresponding frequency of the greatest spectral peak of chaotic signal. By Duffing equation and Chua's circuit, it is proved that the central frequency exists and is determined by the interior parameters of nonlinear system. By adjusting some interior parameters, chaotic signals with different central frequencies can be obtained. it is observed that the central frequency reflects the changing speed of chaotic signal, which means that the faster the chaotic signal evolves, the higher its central frequency is. With the help of the definition of central frequency, the following chapter will quantitatively analyze the effect of chaotic signal on EMI reduction.
Chapter 4 focuses on the effects of central frequency on chaotic modulation. According to the mathematical deduction, chaotic modulation results in the spectral superposition of chaotic signal and normal PWM pulse while spreading the spectrum of PWM pulse. The amplitude of the fundamental component of the switching frequency reaches the greatest value when the central frequency of chaotic signal equals the sawtooth frequency or the switching frequency under chaotic duty modulation. In order to suppress EMI, the central frequency needs to stagger the switching frequency or its multiples. Thus, when the central frequency of chaotic signal is the half of the sawtooth frequencytheir respective spectral peaks exist independently, which implies that EMI reduction becomes the most effective. The chaotic analogue and digital signal generators are designed and built into a DC-DC buck, respectively. Simulations and experimental tests verifies the effect of the central frequency of chaotic signal on suppressing EMI.
Chapter 5 designs a chaotic duty modulation scheme for switching converters and conducts respective experiments. Based on a commercial half-bridge converter, i.e., PC's power supply ATX2.0, chaotic modulation is realized in analogue and digital ways. Simulations and experimental tests verify the design feasibility. Further, comparison is made between the analogue design and the digital one.
Chapter 6 investigates the stability of switching converters under chaotic duty modulation. A switching converter is a typical nonlinear control systemwhose stability refers to regaining the equilibrium once suffering a disturbance according to the classical control theory. In order to analyze the stability, a kinetics model, the circuit average model is adopted, which is accomplished by four steps. Firstly, the average large signal model (ALSM) is established through equivalently averaging the system variables during a switching period. Then, impose the disturbance on ALSM, and construct the direct current model (DCM) and the small signal circuit model (SSCM). Thirdly, the closed-loop transfer function of SSCM is built via Laplace Transform. Finally, on the basis of the transfer function, the conditions of close loop stability are obtained for switching converters under the chaotic duty modulation.
Chapter 7 studies the effects of chaotic modulation on the remaining useful life of switching converters. From the failure modes of switching converters, key components are listed with their failure models including transistor, electrolytic capacitor and rectifier. The further research demonstrates that the output ripples resulting from chaotic modulation influence the remaining useful life of the electrolytic capacitor, which shortens system life. Additionally, once chaotic signal generator runs from chaos status into period, chaotic

modulation fails to suppress EMI effectively, and thus the system performance degrades. Chapter 8 indicates that the effects of chaotic modulation are mainly embodied in input and output characteristics of switching converters. The respective test items and their specifications are listed. Analyses are conducted on experimental results for PC's power supply ATX2.0 under chaotic modulation.
The last chapter draws the conclusions and looks forward to the future work.

2 Circuitry Design for Chaotic Modulation

2.1 Introduction

By normal PWM control, switching converters generate serious electromagnetic interference (EMI) because of the high change rates of voltage and current. Chaotic modulation can be applied to reduce EMI by spreading the discrete EMI energy to a wide frequency band due to the pseudo-randomness and the continuous spectrum characteristics of chaos [34–36]. This chapter presents a qualitative analysis to explain why EMI of switching converts can be suppressed by chaotic frequency modulation and chaotic duty modulation, followed by proposals how to implement chaotic modulation.
The spectrum under chaotic modulation is obtained on the basis of Fourier Transform. Effectiveness of EMI suppression can be evaluated from the frequency spectrum, by which the greater the amplitudes of the fundamental of the switching frequency and harmonics are, the more seriously the system generates EMI. On the contrary, EMI is suppressed if their amplitudes are reduced.
Chaotic modulation has been conducted to reduce EMI in switching converters [30, 36–38], commonly by attaching a disturbance to PWM control module. Taking the voltage-controlled DC-DC buck as an example, this chapter propose the implementation circuits for chaotic frequency modulation and chaotic duty modulation, respectively. The simulation verifies the effectiveness of the proposed schemes.

2.2 Chaotic Frequency Modulation

2.2.1 Principle of Spectrum Spreading

Chaotic frequency modulation makes the cycle vary with a fixed duty. Denote the initial time of the k-th pulse by t_k and the cycle by τ_k. τ_k is described by chaos mapping χ:

$$\tau_k = \chi(\tau_{k-1}), k = 1, 2, 3, ..., \tag{2.1}$$

where $\tau_{k-1} \in (0, 1)$, τ_0 is the initial value of the chaotic series and represents the cycle of the first pulse. The initial time t_{k+1} of the $(k + 1)$-th pulse is

$$t_{k+1} = t_k + \tau_k = t_k + \chi(\tau_{k-1}), k = 1, 2, 3, ..., \tag{2.2}$$

where $\tau_{k-1} \in (0, 1)$. The variable t_0 is the initial time of the transistor driving-pulse, and assume $t_0 = 0$. The variable t_{k+1} is determined by both t_k and τ_k. Therefore, τ_k and t_k are both chaotic series. The transistor driving-pulse are shown in Figure 2.1, where A is the amplitude and D is the duty, both are constant. The product of D and τ_k represents the occupied time of the k-th pulse, and the k-th period of $v(t)$ can be expressed by

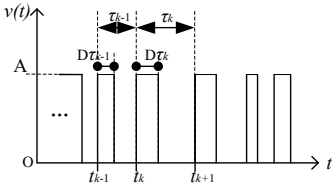


Figure 2.1: Chaotic frequency modulation pulses

$$v_k(t-t_k) = \begin{cases} 0, \ t_k \leq t < t_k + (1-\mathrm{D})\tau_k, \\ \mathrm{A}, \ t_k + (1-\mathrm{D})\tau_k \leq t < t_{k+1}. \end{cases} \tag{2.3}$$

According to Fourier Transform [7], the pulse spectrum denoted by $F_k(t_k, \omega)$ is [39]

$$\begin{aligned} F_k(\tau_k, \omega) &= \int_{t_k}^{t_{k+1}} v_k(t-t_k) e^{-j\omega t} dt \\ &= \int_{t_k}^{t_k+(1-\mathrm{D})\tau_k} v_k(t-t_k) e^{-j\omega t} dt \\ &\quad + \int_{t_k+(1-\mathrm{D})\tau_k}^{t_{k+1}} v_k(t-t_k) e^{-j\omega t} dt \\ &= \int_{t_k+(1-\mathrm{D})\tau_k}^{t_{k+1}} A e^{-j\omega t} dt \\ &= \frac{j\mathrm{A}}{\omega} e^{-j\omega t_{k+1}} [1 - e^{j\omega \mathrm{D}\tau_k}], \end{aligned} \tag{2.4}$$

so the spectrum of $v(t)$ denoted by $F(\omega)$ is

$$\begin{aligned} F(\omega) &= \sum_{k=1}^{+\infty} \frac{j\mathrm{A}}{\omega} e^{-j\omega t_{k+1}} [1 - e^{j\omega \mathrm{D}\tau_k}] \\ &= \frac{j\mathrm{A}}{\omega} \sum_{k=1}^{+\infty} e^{-j\omega t_{k+1}} [1 - e^{j\omega \mathrm{D}\tau_k}]. \end{aligned} \tag{2.5}$$

As shown in Eq. (2.5), the variables t_{k+1} and τ_k are chaotic series, which are of the pseudo-randomness. $F(\omega)$ is the function of t_{k+1} and τ_k, so that $F(\omega)$ has the continuous spectrum. That is, the signal energy of $v(t)$ is spread into a wide frequency range, which results in EMI suppression.

2.2.2 Circuitry Design

The schematic diagram of the voltage-controlled DC-DC converter is shown in Figure 2.2 and it is constituted by two modules. One is the power conversion which is made of the switch Q, the rectifier diode D, the inductor L, and the capacitor C, and the other one is the control module which ensures the closed-loop stability and produces the transistor driving-pulse.

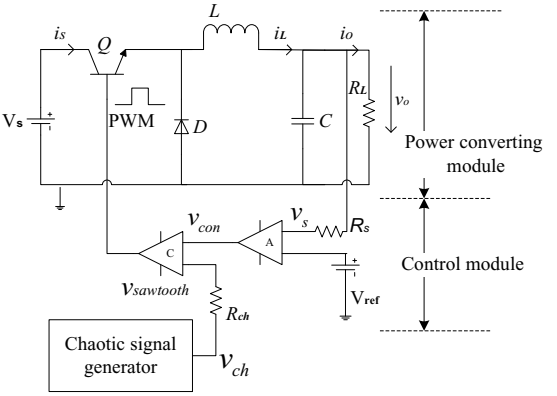


Figure 2.2: The schematic diagram of chaotic frequency modulation

The chaotic signal v_{ch} is processed by the resistor R_{ch}, then the processed signal is connected to the comparator input $v_{sawtooth}$. Denote the proportionality coefficient by k_0, there exists

$$v_{sawtooth} = k_0 v_{ch}. \tag{2.6}$$

Denote the output sampling voltage by v_s and the reference voltage by $\mathrm{V_{ref}}$. The error between v_s and $\mathrm{V_{ref}}$ is amplified to become the control voltage v_{con}. Once the system keeps stable, v_{con} is approximately constant denoted by γ_0. PWM pulse are obtained by comparing v_{con} and $v_{sawtooth}$. Denoting the pulses by z, one can obtain

$$z = \begin{cases} 1, v_{sawtooth} > v_{con}, \\ 0, v_{sawtooth} \leq v_{con}. \end{cases} \tag{2.7}$$

In terms of Eq. (2.6) and $v_{con} \approx \gamma_0$, z can be expressed by

$$z = \begin{cases} 1, v_{ch} > \frac{\gamma_0}{k_0}, \\ 0, v_{ch} \leq \frac{\gamma_0}{k_0}, \end{cases} \tag{2.8}$$

where the cycle τ of the PWM pulse is determined by the signal v_{ch}, which performs chaotic frequency modulation, as shown in Figure 2.3.

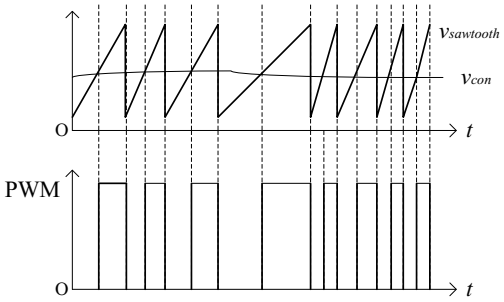


Figure 2.3: Switching pulses of chaotic frequency modulation

2.3 Chaotic Duty Modulation

2.3.1 Principle of Spectrum Spreading

For the chaotic duty modulation, the PWM cycle T_S keeps constant and the duty varies chaotically. Denote the initial time of the k-th pulse by t_k and the duty by d_k. The variable d_k is described by chaos mapping ψ

$$d_k = \psi(d_{k-1}), k = 1, 2, 3, ..., \tag{2.9}$$

where $d_k \in (0, 1)$, d_0 is the initial value of the chaotic series representing the first pulse duty. Denote the pulse amplitude by the constant A. The conduct of d_k and T_S is the occupied time of the k-th pulse, as shown in Figure 2.4. For the k-th period, the PWM function $v(t)$ is defined as [40]

$$v_k(t - t_k) = \begin{cases} 0, \ t_k \le t < t_{k+1} - d_k T_S, \\ A, \ t_{k+1} - d_k T_S \le t < t_{k+1}. \end{cases} \tag{2.10}$$

In terms of Fourier Transform [7], there is

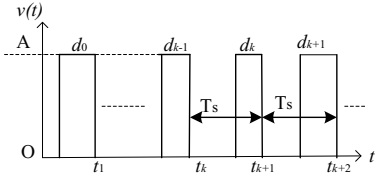


Figure 2.4: The switching pulses under chaotic duty modulation

$$
\begin{aligned}
F_k(d_k,\omega) &= \int_{t_k}^{t_k+\mathrm{T_S}} v_k(t-t_k)e^{-j\omega t}dt \\
&= \int_{t_k}^{t_k+d_k\mathrm{T_S}} v_k(t-t_k)e^{-j\omega t}dt + \int_{t_k+d_k\mathrm{T_S}}^{t_k+\mathrm{T_S}} v_k(t-t_k)e^{-j\omega t}dt \\
&= \int_{t_k}^{t_k+d_k\mathrm{T_S}} Ae^{-j\omega t}dt + \int_{t_k+d_k\mathrm{T_S}}^{t_k+\mathrm{T_S}} 0e^{-j\omega t}dt \\
&= \int_{t_k}^{t_k+d_k\mathrm{T_S}} Ae^{-j\omega t}dt. \qquad (2.11)
\end{aligned}
$$

The cycle $\mathrm{T_S}$ is constant, the initial time of the $(k+1)$-th pulse is $t_{k+1} = (k+2)\mathrm{T_S}$, and $F_k(\omega)$ can be expressed as follows.

$$
\begin{aligned}
F_k(d_k,\omega) &= \int_{(k+2-d_k)\mathrm{T_S}}^{(k+2)\mathrm{T_S}} \mathrm{A}e^{-j\omega t}dt \\
&= -\int_{0}^{d_k\mathrm{T_S}} \mathrm{A}e^{-j\omega t}dt \\
&= \frac{j\mathrm{A}}{\omega}[1-e^{-j\omega d_k\mathrm{T_S}}]. \qquad (2.12)
\end{aligned}
$$

Hence, the spectrum function $F(\omega)$ is

$$
F(\omega) = \sum_{k=1}^{+\infty} \frac{j\mathrm{A}}{\omega}[e^{-j\omega d_k\mathrm{T_S}}-1] = \frac{j\mathrm{A}}{\omega}\sum_{k=1}^{+\infty}[e^{-j\omega d_k\mathrm{T_S}}-1]. \qquad (2.13)
$$

As indicated by the equation (2.9), the pulse duty d_k is a chaotic series. $F(\omega)$ possesses the characteristic of chaos and the continuous spectrum, which implies the EMI reduction.

2.3.2 Circuitry Design

As shown in Figure 2.5, the circuit is demonstrated for the chaotic duty modulation in DC-DC buck converter by injecting the chaotic signal to the PWM module. As the output of the control module, PWM is also expressed by Eq. (2.7).

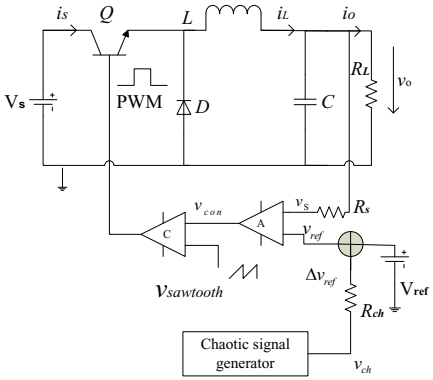


Figure 2.5: The schematic diagram of chaotic duty modulation

The feedback voltage v_S is gotten by sampling the output through the resistor R_S. If the system runs stable, v_S is nearly constant denoted by γ_1. The variable v_{ch} is the external chaotic signal and is linearly processed to be Δv_{ref} through the resistor R_{ch}. Denote the linear coefficient by k_1, there

$$\Delta v_{ref} = k_1 v_{ch}. \tag{2.14}$$

Hence, v_{ref} is

$$v_{ref} = \mathrm{V_{ref}} + \Delta v_{ref}, \tag{2.15}$$

where $\mathrm{V_{ref}}$ is constant, which completes a translation for Δv_{ref}, so v_{ref} reaches a reasonable value range.

The variable v_{con} is the control voltage, which is the issue of amplifying the error between v_S and v_{ref}. Assume that the amplifier gain is constant, and denote the gain by $\mathrm{A_1}$. The variable v_{con} is described by

$$v_{con} = \mathrm{A_1}(v_S - v_{ref}) = \mathrm{A_1}(\gamma_1 - \mathrm{V_{ref}}) - \mathrm{A_1} k_1 v_{ch}, \tag{2.16}$$

where includes two parts. One part of the equation is $\mathrm{A_1}(\gamma_1 - \mathrm{V_{ref}})$, which is constant denoted by γ_2. The other one is $\mathrm{A_1} k_1 v_{ch}$, and the product of $\mathrm{A_1}$ and k_1 is constant, which is denoted by γ_3. Therefore, v_{con} is simplified as

$$v_{con} = \gamma_2 + \gamma_3 v_{ch}. \tag{2.17}$$

Define the sawtooth as

$$v_{sawtooth} = \mathrm{V_L} + (\mathrm{V_U} - \mathrm{V_L})(\frac{t}{\mathrm{T_s}} mod 1), \tag{2.18}$$

where $\mathrm{V_L}$ and $\mathrm{V_U}$ are the minimum and maximum values respectively, and $\mathrm{T_s}$ is the cycle of the sawtooth.
As depicted by the preceding, v_{con} is the result of processing v_{ch} by the linear transformation and translation, therefore, v_{con} persists the chaotic characteristic of v_{ch}. PWM is further expressed

$$z = \begin{cases} 1, v_{sawtooth} > \gamma_2 + \gamma_3 v_{ch}, \\ 0, v_{sawtooth} \leq \gamma_2 + \gamma_3 v_{ch}. \end{cases} \tag{2.19}$$

Hence, v_{con} and $v_{sawtooth}$ work together to produce PWM pulses. The pulse cycle is the same as the cycle of $v_{sawtooth}$, but the duty is determined by v_{con} and $v_{sawtooth}$. In essence, the duty varies along with v_{ch}, which means realizing the chaotic duty modulation, as shown in Figure 2.6.

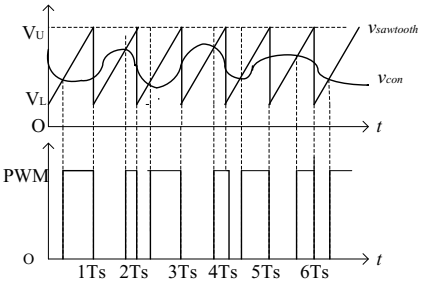
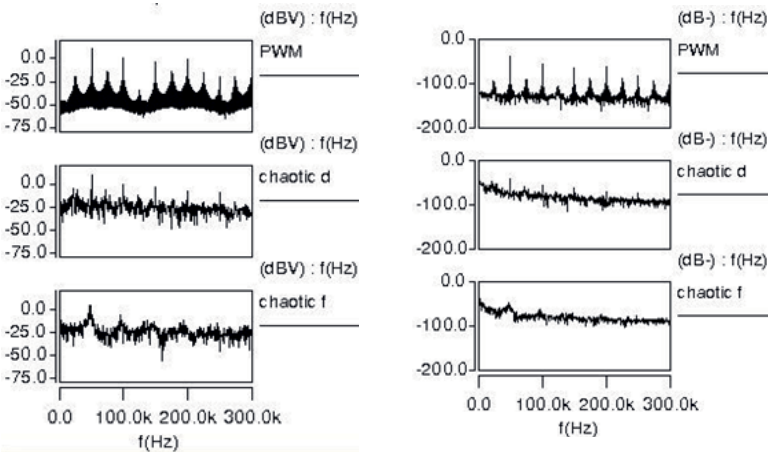


Figure 2.6: Switching pulses of chaotic duty modulation

2.4 Simulations

In terms of Figures 2.2 and 2.5, simulations are conducted by the software Saber. Assume that $\mathrm{U_S}$=28 V, f_S=50 kHz, R_L = 1 Ω, L=1 mH, C=470 uF and the power switch model is IRF130_sl2. Comparisons are conducted among the normal PWM, chaotic duty modulation and chaotic frequency modulation. In order to keep the system stable and obtain the best effect, the chaotic signal with the central frequency 25 kHz is applied in chaotic

duty modulation, while the chaotic signal with the central frequency 48 kHz in chaotic frequency modulation.
FFT of PWM pulse and inductor current are demonstrated in Figure 2.7. Table 2.1 lists the amplitudes of the fundamental component and harmonics under three cases. It can be found that the peaks at the fundamental and harmonics are smoothed under chaotic modulation, which means the EMI suppression. For PWM pulse, under normal PWM control, chaotic duty modulation and chaotic frequency modulation, the amplitudes of its fundamental component are -39.2 dB, -40.8 dB and -45 dB, respectively. From the viewpoint of EMI reduction, chaotic frequency modulation is more effective than chaotic duty modulation, however, more serious output ripples occur under chaotic frequency modulation, as shown in Figure 2.8.



(a) FFT of the transistor driving-pulse

(b) FFT of the inductor current

Figure 2.7: FFT waveforms (Upper: normal PWM, middle: chaotic duty modulation, lower: chaotic frequency modulation)

2.5 Summary

Chaotic frequency modulation and chaotic duty modulation have been respectively analyzed for suppressing EMI. The respective implementation circuit for DC-DC buck converter has been proposed. Chaotic modulation has been performed by injecting the chaotic signal into the PWM control module. According to the simulation results, these two types of chaotic modulations can smooth the peaks of the fundamental of the switching frequency

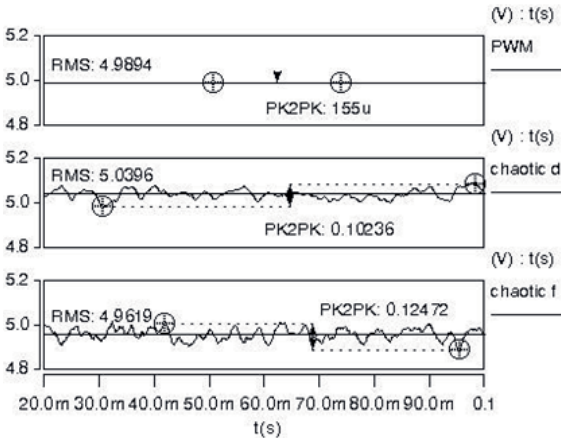


Figure 2.8: Output ripples

Table 2.1: The amplitudes of inductor currents under the different PWM controls

	f_S	$2f_S$	$3f_S$	$4f_S$	$5f_S$	$6f_S$
Normal PWM	-39.2	-54.5	-63	-63	-72	-70
Chaotic frequency	-45	-62	-70	-73	-78	-80
Chaotic duty	-40.8	-57	-64	-70	-72	-73

and harmonics and reduce EMI. In the meantime, the output ripple under the chaotic duty modulation is less than that under the chaotic frequency modulation.

3 Central Frequency of Chaotic Signals

3.1 Introduction

Chaotic modulation has been widely applied in the security communication, the EMI suppression of power electronics and so on [34–36], because the spectrum can be spread through chaotic modulation due to the pseudo-randomness and the continuous spectrum characteristics of chaos. Some researches [20, 22, 33] have probed that the effectiveness of EMI suppression is related to the spectral characteristics of the chaotic signal used by the chaotic modulation.

The spectral characteristics of chaotic signal mainly refers to the spectral distribution, i.e. spectral peaks and width. Factually, with some peaks and a limited spectral rangespectral curve of chaotic signal is not smooth, which makes itself a non-ideal wide spectrum signal [41]. In order to analyze quantitatively, this study defines the central frequency of chaotic signal as the frequency corresponding to the greatest spectral peak of chaotic signal, denoting the central frequency as f_o.

A chaotic signal is produced by some deterministic rules [42], which are categorized into discrete chaos mapping systems and continuous chaos systems. Under certain conditions, some discrete nonlinear mapping systems generate the chaotic series, like Logistic map, Henon map and Tent map. The continuous chaos system is commonly described by a nonlinear differential equation, presenting that the chaotic signal is continuous on its amplitude and time. The systems are classified into the non-autonomous system and the autonomous one according to the relation between system status and time.

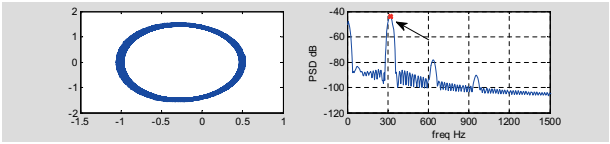
This chapter mainly focuses on central frequencies of chaotic signals produced by a non-autonomous system and an autonomous one, respectively, taking the Duffing oscillator as the example of non-autonomous system and Chua's circuit as the example of an autonomous one.

3.2 Duffing Oscillator

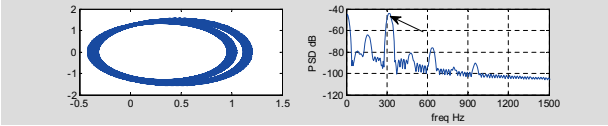
The Duffing equation describes the status of an elastic system under the external periodic force [43], as shown in Eq. (3.1).

$$\ddot{x} + a\dot{x} + kx + \mu x^3 = F\cos(\omega t), \tag{3.1}$$

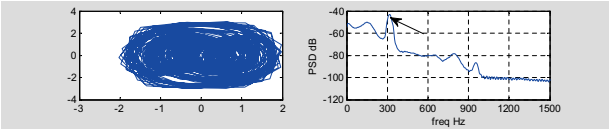
where F and ω are amplitude and angular frequency of the external periodic force, respectively. a, k and μ are constant coefficients of elastic system. Given k=1, μ=1, a=-0.5, and the initial values of $\ddot{x}$ and $\dot{x}$ stand for -0.1, simulation is conducted with Matlab software. Firstly, keep ω constant and enable F changeable. Here, let ω=2, then the trajectories and power spectrum curves of Duffing elastic system are shown in Figure 3.1.



(a) F=3.5



(b) F=3.25



(c) F=3.0

Figure 3.1: The system trajectory and the PSD of the signal when ω=2

Once F is changed, the elastic system status evolves among the period, multi-period and chaos, as demonstrated in Figure 3.1.

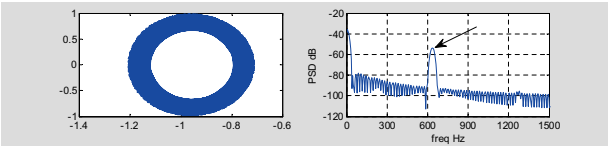
When F=3.5, the system appears periodic and the trajectory is close-loop. There are three distinct peaks on the signal power spectrum curve. The fundamental component f_1 is highlighted by an arrow in this figure, and the adjacent peaks refer to the 2nd. and the 3rd. component denoted by $2f_1$, $3f_1$, respectively.

When F=3.25, the system runs into bi-period. The signal power spectrum curve appears multiple components like $0.5f_1$, f_1, $1.5f_1$, $2f_1$, $2.5f_1$ and $3f_1$.

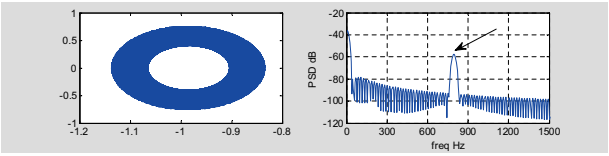
When F=3.0, the system displays chaotic. The signal power spectrum curve flattens its peaks, but the component f_1 still remains its greatest peak.

Then, keep F constant and change the value of ω. The trajectories and power spectrum curves can be seen in Figure 3.2 when ω is equal to 4, 5 and 6, respectively. Each power spectrum curve has a distinct peak located at the fundamental component. Along with increasing ω, the frequency of the fundamental component increases.

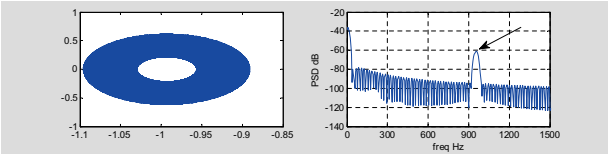
Thus, Duffing elastic system develops in many statuses like single-period, multi-period and chaos when the amplitude of the external force varies. However, the frequency of the fundamental component is invariant on the signal power spectrum curve as long as the angular frequency ω of external force keeps constant. On the contrary, when the amplitude of external force keeps constant and the angular frequency ω varies, the system behaviour can be changed from period to chaos. The frequency of fundamental component varies along with ω, on which the greatest spectral peak appears.



(a) ω=4



(b) ω=5



(c) ω=6

Figure 3.2: The system trajectory and the PSD of the signal while changing ω

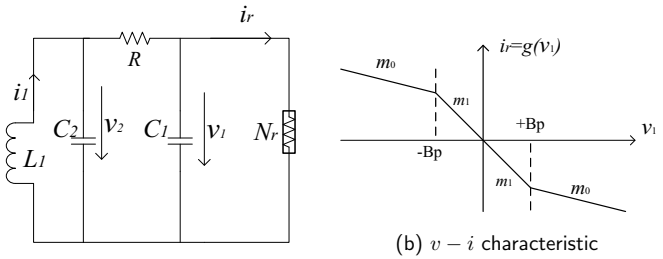
3.3 Chua's Circuit

Chua's circuit is composed of a sine oscillator and a voltage-controlled nonlinear resistor [42], which includes three energy storage elements, an inductor and two capacitors. Figure 3.3 (a) shows Chua's circuit, in which we denote i_1 as the current through the inductor L_1, v_1 and v_2 as the voltages across the capacitors C_1 and C_2. Figure 3.3 (b) presents the $v-i$ characteristic curve of the nonlinear resistor N_r, which is piecewise linear function with the outer line slope m_0, the internal line slope m_1, and the abscissas $+\mathrm{B_P}, -\mathrm{B_P}$ of the two breakpoints. Chua's circuit is expressed by the following equations (3.2).

$$\begin{cases} \frac{\mathrm{d}v_1}{\mathrm{d}t} = \frac{1}{C_1}[(v_2 - v_1)G - f(v_1)], \\ \frac{\mathrm{d}v_2}{\mathrm{d}t} = \frac{1}{C_2}[(v_1 - v_2)G + i_1], \\ \frac{\mathrm{d}i_1}{\mathrm{d}t} = \frac{1}{L_1}v_2, \end{cases} \tag{3.2}$$

where $G = \frac{1}{R}$, $f(v_1)$ is the current i_r through N_r, which is the function of v_1. It can be expressed as

$$f(v_1) = m_0 v_1 + 0.5(m_1 - m_0)[|v_1 + \mathrm{B_P}| - |v_1 - \mathrm{B_P}|]. \tag{3.3}$$



(a) Chua's circuit

(b) $v - i$ characteristic

Figure 3.3: Chua's circuit and the characteristic of the nonlinear resistor

3.3.1 Unitary Processing

A unitary processing is made for the equations (3.2) and (3.3). Set the parameters as follows [44].

$$\begin{aligned} x = \frac{v_1}{\mathrm{B_P}}, y = \frac{v_2}{\mathrm{B_P}}, z = \frac{Ri_1}{\mathrm{B_P}}, \tau = \frac{t}{RC_2}, \\ \alpha' = \frac{C_2}{C_1}, \beta' = \frac{C_2 R^2}{L_1}, a = Rm_1, b = Rm_0. \end{aligned} \tag{3.4}$$

The dimensionless equations (3.5) is obtained for Chua's circuit.

$$\begin{cases} \frac{dx}{d\tau} = \alpha'(y - x - f(x)), \\ \frac{dy}{d\tau} = x - y + z, \\ \frac{dz}{d\tau} = -\beta' y, \end{cases} \tag{3.5}$$

where

$$f(x) = bx + 0.5(a - b)[|x + 1| - |x - 1|], \tag{3.6}$$

and the function (3.6) is three segment linear, which has two slopes of a and b.
For the equations (3.5) and (3.6), simulations are conducted under the parameter set: $\alpha' = 9.0$, $\beta' = 14.87$, $a = -1.183$ and $b = -2.3114$. The evolving waveform of v_2 and the trajectory of $v_2 - v_1$ are shown in Figure 3.4.
It can be seen that Chua's circuit holds the chaotic behavior as long as the parameter set remains invariant. According to the equation (3.4), there is no effect on α', β', a and b when increasing or decreasing C_1, C_2 and L_1 simultaneously.

3.3.2 The Oscillating Frequency

The equation (3.6) can be described as a third-order linear polynomial function, which is the complex frequency domain as expressed [45],

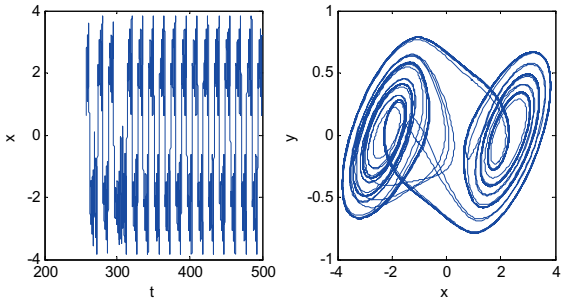


Figure 3.4: The chaotic signal of Chua's circuit and the trajectory of $v_2 - v_1$

$$s^3 + q_2 s^2 + q_1 s + q_0 = 0, \tag{3.7}$$

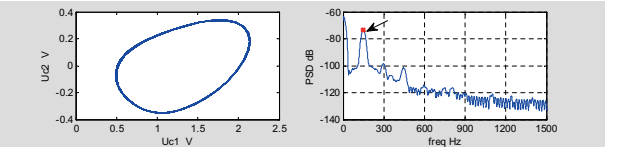
where s is the complex frequency, q_0, q_1 and q_2 are determined by C_1, C_2, G, L_1 and $m_i (i = 0, 1)$. That is, $q_0 = \frac{G+m_i}{L_1 C_1 C_2}$, $q_1 = \frac{1}{L_1 C_2} + \frac{G+m_i}{C_1 C_2}$, $q_2 = \frac{G}{C_2} + \frac{G+m_i}{C_1}$.
When the oscillator of Chua's circuit runs in sine periodic status, the oscillating frequency remains at a constant value, on which the energy concentrates. Hence, the spectrum of oscillating signal is discrete. The component of oscillating frequency is demonstrated in Figure 3.5 (a). According to the oscillating condition, the oscillating frequency of Chua's circuit is estimated as [45],

$$f = \frac{1}{2\pi\sqrt{L_1 C_2}} \sqrt{1 + \frac{G L_1 m_i}{C_1}}, i = 0, 1. \tag{3.8}$$

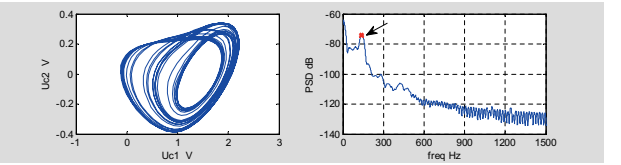
Once Chua's circuit runs into chaotic status, the energy is scattered at each component. However, the energy is relatively concentrated on the limited scope centered the oscillating frequency, as displayed in Figure 3.5 (b).

3.4 Central Frequency

From the above analysis of Duffing oscillator and Chua's circuit, the nonlinear systems run from period to chaotic status under certain conditions. Consequently, the signal spectrum curves vary, but a distinct peak locates at the fundamental component. For Duffing oscillator, the fundamental frequency is determined by the angular frequency of external force. For Chua's circuit, the fundamental frequency is the oscillating frequency, which is determined by device parameters. The fundamental frequency is just the central frequency f_o of chaotic signal determined by the interior parameters of the system.
In Duffing elastic system, f_o is the fundamental frequency of chaotic signal, which is influenced by the angular frequency ω. As a result, the greater ω, the greater f_o. Figure 3.6 shows the evolving waveforms of Duffing chaotic signals under two different ω. The evolving



(a) Period

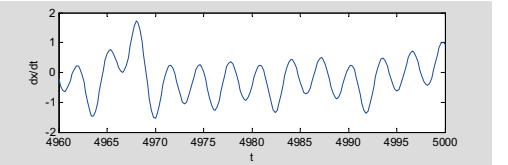


(b) Chaos

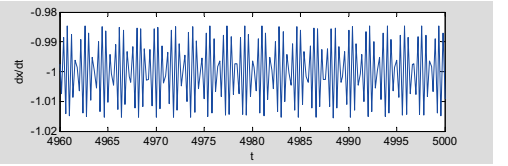
Figure 3.5: The trajectory of Chua's circuit and the PSD of the signal

speed is higher when ω=14 than when ω=2. Figure 3.7 exhibits two sets of chaotic signals and their spectra produced by Chua's circuit simulated by Saber 7.0. One is about the central frequency f_o=12.4 kHz, the other is about f_o=24 kHz.

In short, the central frequency f_o is an attribute of chaotic signal and describes its evolving speed, which is corresponding to the greatest spectral component of chaotic signal.

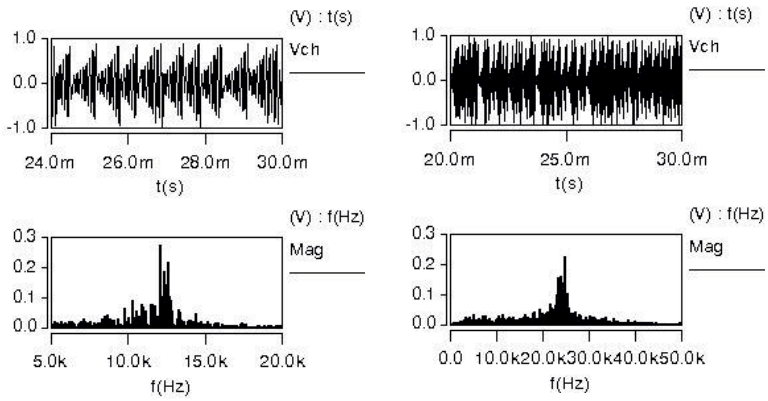


(a) F=3.0 ω=2



(b) F=3.0 ω=14

Figure 3.6: The evolving waveform of the chaotic signal in Duffing system



(a) $C_1 : 2.45\text{nF}, C_2 : 22.7\text{nF}, L_1 : 5\text{mH}$ (b) $C_1 : 1.20\text{nF}, C_2 : 11.2\text{nF}, L_1 : 2.5\text{mH}$

Figure 3.7: The chaotic signals of Chua's circuit (upper)and their spectra (lower)

3.5 Summary

The study has been developed through Duffing oscillator and Chua's circuit that the nonlinear system would be oscillating around the central frequency once it shows the chaotic behavior. The central frequency is defined as the frequency corresponding to the greatest spectral peak of chaotic signal. Meanwhile, the central frequency reflects the changing speed of chaotic signal. In the following chapter, the further study is to explore the effect of the central frequency on EMI reduction in switching converters under chaotic modulation.

4 Effect of Central Frequency on EMI Reduction

Chaotic signals have the characteristics of fluctuant and continuous spectrum waveform due to the pseudo-randomness of chaos. The frequency corresponding to the largest spectral peak of a chaotic signal is defined as the central frequency in the previous chapter. This chapter is concerned with the effect of the central frequency on chaotic modulation. As one kind of spread spectrum modulation, the chaotic duty modulation is adopted to suppress electromagnetic interference (EMI) in switching converters. Simulations and experiments are conducted to verify the idea on a DC-DC buck converter. In terms of the central frequency, whether the chaotic signal being the most optimal for chaotic modulation or not can be estimated.

4.1 Introduction

Due to the pseudo-randomness and continuous spectrum of chaos, chaotic modulation has been widely applied in the security communication, the EMI reduction of power electronics and so on [34–36]. However, the spectrum waveform of chaos is fluctuant with some peaks and the energy concentrates upon a limited range of frequency [41]. It is reported in [46] that the spectrum range of the chaotic signal is required to match the actual bandwidth of the communication channel in the security communication. In another paper [22], a chaotic frequency modulation has been implemented to reduce EMI by connecting external Chua's chaotic signal to the PWM module of a DC-DC boost converter, and the chaotic oscillating frequency is required to approach the switching frequency of the converter. Therefore, the effectiveness of chaotic modulation is related to the spectral characteristics of chaotic signal.

As an attribute of chaotic signal, its central frequency f_o has been defined as the frequency corresponding to the the largest spectral peak in Chapter 3. In this chapter, on the basis of Fourier Transform, the spectrum expressions are derived for the normal PWM signal and the chaotic duty modulation signal, respectively. It is certified that the PWM spectrum under chaotic modulation is continuous in the frequency and the amplitude, for which the spectral amplitudes of the fundamental component and its harmonics are affected by the central frequency of the chaotic signal. Based on Chua's circuit, the simulation and the experimental results indicate that the optimal central frequency is related to the switching frequency f_s. Meanwhile, an algorithm is designed to produce the chaotic signal from the discrete chaos map. A chaotic digital signal generator is realized through embedding the micro-controller unit (MCU) or micro-processor unit (MPU) into the system, on which the simulation and experimental tests are verified that the central frequency has an effect on the EMI suppression.

4.2 Frequency Spectrum under Chaotic modulation

The voltage-controlled PWM module has been taken as an example, in which an oscillator generates the periodic sawtooth waves. The following is about the PWM spectrum under the chaotic duty control.

4.2.1 Chaotic Duty Modulation

As shown in Figure 2.5, the circuit is demonstrated for the chaotic duty modulation in a DC-DC buck converter by injecting the chaotic signal to the PWM module.
The variable v_{ch} is the external chaotic signal and is linearly processed to be Δv_{ref} through the resistor R_{ch}. Denote the linear coefficient by k_1, there

$$\Delta v_{ref} = k_1 v_{ch}. \tag{4.1}$$

The variable v_{con} is the control voltage. It is the issue of amplifying the error between v_S and v_{ref}. Assume that the amplifier gain is constant and denoted by A_1. The variable v_{con} is described by

$$v_{con} = \mathrm{A}_1(v_S - v_{ref}) = \mathrm{A}_1(\gamma_1 - \mathrm{V}_{\mathrm{ref}}) - \mathrm{A}_1 k_1 v_{ch}, \tag{4.2}$$

which includes two parts. One part of the equation is $\mathrm{A}_1(\gamma_1 - \mathrm{V}_{\mathrm{ref}})$, which is constant and denoted by γ_2. The other one is $\mathrm{A}_1 k_1 v_{ch}$, where $\mathrm{A}_1 k_1$ is constant and denoted by γ_3. Therefore, v_{con} is simplified as

$$v_{con} = \gamma_2 + \gamma_3 v_{ch}. \tag{4.3}$$

Because v_{con} is the result of processing v_{ch} by linearization and translation, v_{con} is also chaotic and the duty of the modulation pulse is consequently chaotic, as shown in Figure 4.1.

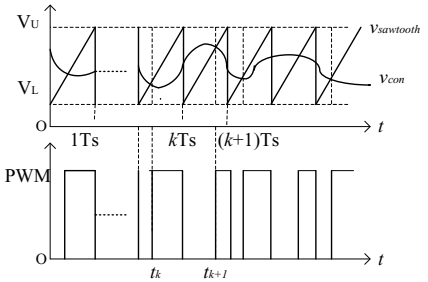


Figure 4.1: Waveforms of $v_{sawtooth}, v_{con}$ and chaotic modulation pulse

4.2.2 Spectral Analysis

Define the sawtooth as

$$v_{sawtooth} = \mathrm{V_L} + (\mathrm{V_U} - \mathrm{V_L})(\frac{t}{\mathrm{T_s}} mod 1), \tag{4.4}$$

where $\mathrm{V_L}$ and $\mathrm{V_U}$ are the minimum and the maximum respectively, and $\mathrm{T_s}$ is the cycle of the sawtooth. In Figure 4.1, high-level initial time t_k of the kth pulse is determined by the crosspoint of v_{con} and $v_{sawtooth}$:

$$\begin{aligned} t_k &= (k-1)\mathrm{T_s} + \frac{v_{con} - \mathrm{V_L}}{\mathrm{V_U} - \mathrm{V_L}}\mathrm{T_s} \\ &= (k-1)\mathrm{T_s} + \frac{\gamma_3 v_{ch} + \gamma_2 - \mathrm{V_L}}{\mathrm{V_U} - \mathrm{V_L}}\mathrm{T_s}. \end{aligned} \tag{4.5}$$

Denote v_{ch} at the crosspoint by $v_{ch}(k)$ in the kth cycle. In terms of Fourier transform [7], the spectrum for the kth pulse is expressed as

$$F_k(\omega) = \int_0^{k\mathrm{T_s}-t_k} \mathrm{A}e^{-j\omega t}dt = \frac{j\mathrm{A}}{\omega}[e^{-j\omega(k\mathrm{T_s}-t_k)} - 1], \tag{4.6}$$

further, the equation (4.6) can be rewritten as

$$F_k(\omega) = \frac{j\mathrm{A}}{\omega}\left[e^{-j\omega\left(\mathrm{T_s}-\left(\frac{\gamma_3 v_{ch}(k)+\gamma_2-\mathrm{V_L}}{\mathrm{V_U}-\mathrm{V_L}}\mathrm{T_s}\right)\right)} - 1\right]. \tag{4.7}$$

Assume $\frac{\gamma_3 v_{ch}+\gamma_2-\mathrm{V_L}}{\mathrm{V_U}-\mathrm{V_L}} = \mu v_{ch} + b_1$, then $\mu = \frac{\gamma_3}{\mathrm{V_U}-\mathrm{V_L}} > 0$, and $b_1 = \frac{\gamma_2-\mathrm{V_L}}{\mathrm{V_U}-\mathrm{V_L}} > 0$. The equation (4.7) can be expressed as

$$F_k(\omega) = \frac{j\mathrm{A}}{\omega}\left[e^{-j\omega\mathrm{T_s}(1-\mu v_{ch}(k)-b_1)} - 1\right]. \tag{4.8}$$

Hence, the spectrum of chaotic modulation pulse denoted by $F(\omega)$ is

$$F(\omega) = \sum_{k=1}^{+\infty} \frac{j\mathrm{A}}{\omega}\left[e^{-j\omega\mathrm{T_s}(1-\mu v_{ch}(k)-b_1)} - 1\right]. \tag{4.9}$$

From Eq. (4.9), the $F(\omega)$ is a continuous function because of the chaotic PWM pulse. EMI peaks of the converter are commonly known at the fundamental component and its harmonics of the switching frequency, so $F(\omega)$ have the extremal points. Denote $n\omega_1$ as angular frequency of the nth harmonic (n is a integer, it represents the fundamental when $n = 1$, otherwise it represents the harmonics). According to the equation (4.9), the fundamental and the harmonics can be expressed as

$$\begin{aligned} F(\omega_n) &= \sum_{k=1}^{+\infty} \frac{j\mathrm{A}}{\omega_n}\left[e^{-j2n\pi(1-\mu v_{ch}-b_1)} - 1\right] \\ &= \sum_{k=1}^{+\infty} \frac{j\mathrm{A}}{\omega_n}\left[e^{-j2n\pi}e^{j2n\mu v_{ch}(k)\pi}e^{j2nb_1\pi} - 1\right], \end{aligned} \tag{4.10}$$

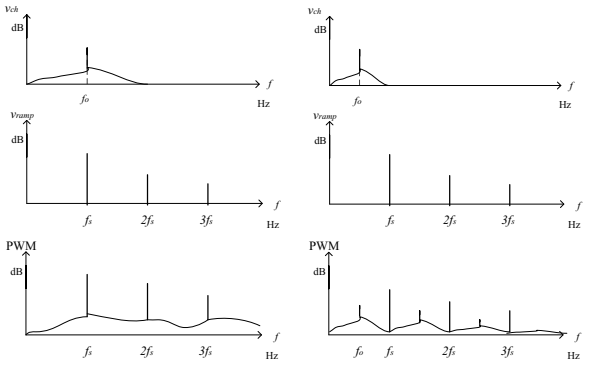
where $e^{-j2n\pi}$ and $e^{j2nb_1\pi}$ are constant, $e^{j2n\pi\mu v_{ch}(k)}$ is variable, and $F(\omega_n)$ varies along with $v_{ch}(k)$. Because $F(\omega_n)$ is the extremal point, there exists extremal values at the fundamental and the harmonics for $e^{j2n\pi\mu v_{ch}(k)}$. In terms of the extremal conditions, one can get $\frac{d(e^{j2n\pi\mu v_{ch}(k)})}{d\omega} = 0$, and $\frac{d^2(e^{j2n\pi\mu v_{ch}(k)})}{d\omega^2} < 0$. Further,

$$\frac{d\left(e^{j2n\pi\mu v_{ch}(k)}\right)}{d\omega} = j2n\pi\mu e^{j2n\pi\mu v_{ch}(k)}\frac{dv_{ch}(k)}{d\omega}, \tag{4.11}$$

$$\begin{aligned}\frac{d^2\left(e^{j2n\pi\mu v_{ch}(k)}\right)}{d\omega^2} &= -(2n\pi\mu)^2 e^{j2n\pi\mu v_{ch}(k)}\left(\frac{dv_{ch}(k)}{d\omega}\right)^2 \\ &+ j2n\pi\mu e^{j2n\pi\mu v_{ch}(k)}\frac{d^2v_{ch}(k)}{d\omega^2}.\end{aligned} \tag{4.12}$$

When $\frac{dv_{ch}(k)}{d\omega} = 0$, the equation (4.11) becomes 0. When $\frac{dv_{ch}(k)}{d\omega} = 0$ and $\frac{d^2v_{ch}(k)}{d\omega^2} < 0$, Eq. (4.12)<0. Therefore, when v_{ch} spectrum obtains the extremal values at the fundamental component of the switching frequency and its harmonics, the modulation pulse spectrum reaches the extremal value. Hence, at the fundamental and the harmonics, v_{ch} spectrum maximizes, so does $F(\omega_n)$ spectrum.

The frequency of the chaotic signal spectrum peak has been defined by central frequency, which is denoted by f_o. Hence, the fundamental component and its harmonics of the modulation pulse maximize when f_o equals the switching frequency f_s, as shown in Figure 4.2 (a). In order to smooth the spectrum peaks of the modulation pulse to suppress EMI, f_o should be deviated from the fundamental and the harmonics of the switching frequency, for example, $f_o = (0.5 + n)f_s, n = 0, 1, 2....$ Figure 4.2 (b) is for $f_o = 0.5f_s$.



(a) $f_o = f_s$ (b) $f_o = 0.5f_s$

Figure 4.2: Illustration for spectra of v_{ch} (upper),$v_{sawtooth}$ (middle) and driving-pulse (lower)

Table 4.1: Combinations of parameters and the relative central frequency

parameters	f_o(kHz)
$C_1 = 44$ nF, $C_2 = 396$ nF, $L_1 = 88$ mH	0.7
$C_1 = 22$ nF, $C_2 = 198$ nF, $L_1 = 44$ mH	1.4
$C_1 = 11$ nF, $C_2 = 99$ nF, $L_1 = 22$ mH	2.8
$C_1 = 5.5$ nF, $C_2 = 49.5$ nF, $L_1 = 11$ mH	5.6
$C_1 = 2.7$ nF, $C_2 = 25$ nF, $L_1 = 5.5$ mH	11.2
$C_1 = 2.45$ nF, $C_2 = 22.7$ nF, $L_1 = 5$ mH	12.5
$C_1 = 1.70$ nF, $C_2 = 15.8$ nF, $L_1 = 3.5$ mH	17
$C_1 = 1.45$ nF, $C_2 = 13.5$ nF, $L_1 = 3$ mH	20.5
$C_1 = 1.20$ nF, $C_2 = 11.2$ nF, $L_1 = 2.5$ mH	24
$C_1 = 0.95$ nF, $C_2 = 9.0$ nF, $L_1 = 2$ mH	29
$C_1 = 0.80$ nF, $C_2 = 7.65$ nF, $L_1 = 1.7$ mH	34.57
$C_1 = 0.76$ nF, $C_2 = 7.20$ nF, $L_1 = 1.65$ mH	36

4.3 Chaotic Analogue Signal

4.3.1 Parameter Configuration for Central Frequency

Chaotic analogue signal generator usually applies Chua's circuit and its improved circuits [17, 37]. According to the equation (3.4) in Chapter 2, the system still runs in chaos while adjusting the capacitors C_1, C_2 and the inductor L_1 as well as remaining the parameters α', β', a and b unchanged [44]. For a practical circuit scheme, each component is selected according to its nominal values, so the theoretical values of C_1, C_2 and L_1 are adjusted slightly in accordance with their nominal value. From the equation (3.8), different central frequency can be obtained by adjusting the parameters of C_1,C_2 and L_1 [44]. Table 4.1 lists some sets of parameter combinations and the respective center frequencies. The analysis is conducted on a DC-DC buck converter as shown in Figure 2.5. According to Eq. (2.7), the chaotic duty modulation is realized with two analogue signals acting as the inputs of the comparator, which produces the chaotic duty pulses. Once the system generates the steady output voltage, v_{con} is expressed by Eq. (4.3) in case of γ_2 and γ_3 being constant. Hence, v_{con} is the result of the linearization and the translation of v_{ch}. The values of γ_2 and γ_3 make the period of v_{con} as same as the period of v_{ch}, which keep the frequency character unchanged after the linearization and the translation. Figure 4.3 shows the evolving waves of the control voltage v_{con}, the sawtooth and the chaotic duty pulse, respectively.

4.3.2 Simulations and Experiments

a. Simulations

Based on Figure 2.5, the parameters are listed as follows: $R_L = 1\ \Omega, L = 1$ mH, $C = 470$ uF, $\alpha' = 0.25, \mathrm{V_L} = 0$ V, $\mathrm{V_U} = 3$ V, $\mathrm{V_s} = 25$ V, $\mathrm{V_{ref}} = 2.4$ V, $R_{ch} = 10$ kΩ. The sawtooth oscillating frequency of PWM module is set up at 48 kHz, so the switching

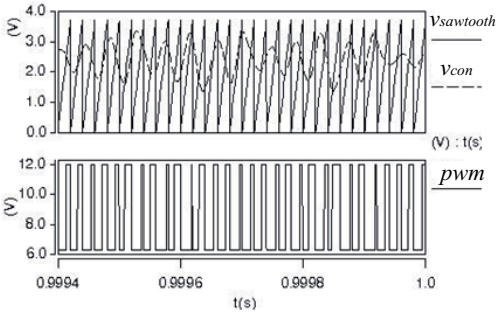


Figure 4.3: Chaotic duty modulation

Table 4.2: The amplitudes of the fundamental component (unit:dB)

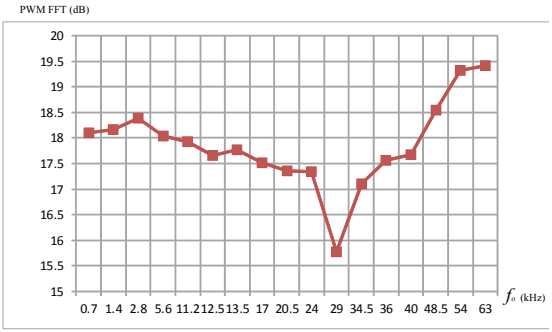
f_O (kHz)	0.7	1.4	2.8	5.6	11.2	12.5	13.5	17	20.5
PWM FFT	18.10	18.17	18.38	18.04	17.93	17.66	17.77	17.52	17.36
i_L FFT	-39.40	-39.84	-39.89	-40.29	-40.34	-40.36	-40.43	-40.82	-40.92
f_O (kHz)	24	29	34.5	36	40	48.5	54	63	no chaos
PWM FFT	17.34	15.78	17.11	17.57	17.67	18.55	19.32	19.41	19.22
i_L FFT	-41.10	-41.89	-40.93	-40.68	-39.56	-39.56	-38.60	-38.43	-38.78

frequency f_s is 48 kHz. When the system is controlled by the normal PWM without chaotic modulation, the resistor R_{ch} is disconnected. When the system is controlled by chaotic PWM, the external chaotic signal v_{ch}, which is drawn from the voltage v_2 of Chua's circuit, is connected to the resistor R_{ch}.

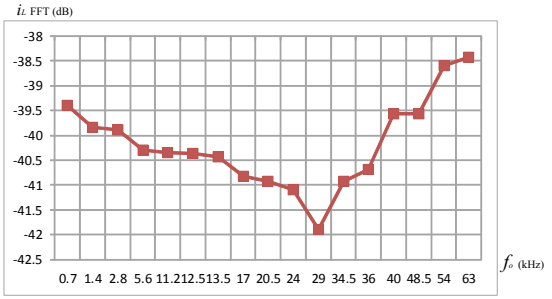
Simulations are conducted to compare EMI reduction effects with different center frequencies of chaotic signals. The parameters of Chua's circuit are set up according to Table 4.1. Taking the amplitude of the fundamental component as the object, Table 4.2 lists the values about the PWM and the inductor current under different center frequencies. Further, it can be also observed in Figure 4.4 that FFT fundamental amplitudes vary along with the central frequency. The lowest value appears when $f_o \approx 0.5 f_s$, which means the optimal EMI suppression.

b. Experimental Results

The scheme in Figure 2.5 is realized by hardware. Assume $R_L = 1\ \Omega, L = 1$ mH, $C = 470$ uF, $\mathrm{V_L} = 0$ V, $\mathrm{V_U} = 3$ V, $\mathrm{V_s} = 25$ V, $\mathrm{V_{ref}} = 2.4$ V, $R_{ch} = 10$ kΩ, and the switching frequency $f_s = 25$ kHz. Chaotic signals with $f_o = 24$ kHz and $f_o = 12.5$ kHz are respectively produced by adjusting the parameters of C_1, C_2 and L_1 in Chua's circuit according to Table 4.1. PWM waveforms and their spectra are shown in Figure 4.5. It can be observed that the amplitudes of the fundamental and harmonics are reduced more when $f_o = 12.5$ kHz than when $f_o = 24$ kHz.



(a) Fundamental amplitudes of PWM FFTs



(b) Fundamental amplitudes of i_L FFTs

Figure 4.4: The central frequency vs the amplitude of the fundamental

(a) $f_o = 12.5$ kHz

(b) $f_o = 24$ kHz

Figure 4.5: The experimental waveforms for transistor driving-pulse

4.4 Chaotic Digital Signal

4.4.1 Chaotic Maps

A chaotic signal can be generated by some various means which sre categorized into the analogue and the digital, but an analogue chaos circuit is infamous for the questions of parameter drift and parameter adjusting. Compared with chaotic analogue signal generator, the digital one possesses two advantages for using the chaos map to produce the chaotic signal. One is adjusting parameters easily by programming, the other one is the code remaining unchanged once burned into the chip.
There are some typical chaotic maps such as Logistic map, Henon map and Tent map, which are listed as follows.
1. Logistic map:

$$\begin{aligned} x_{n+1} &= ax_n(1-x_n), \\ 3.5699456 < a \leq 4, n &= 1,2,3,\ldots\ x_n \in (0,1). \end{aligned} \tag{4.13}$$

2. Henon map:

$$\begin{aligned} &\begin{cases} x_{n+1} = y_{n+1} - ax_{n+1}^2, \\ y_{n+1} = bx_n, \end{cases} \\ a \in (0,1.4), 0.2 < b \leq 0.314, &n = 1,2,3,\ldots \end{aligned} \tag{4.14}$$

3. Tent map

$$\begin{aligned} x_{n+1} &= a - (1+a)|x_n|, \\ a \in (0,1), n &= 1,2,3,\ldots\ x_n \in (0,1). \end{aligned} \tag{4.15}$$

To generate the chaotic signal based on the chaos map, the following steps are demanded to complete. Firstly, design the algorithm to make the signal chaotic. Then, on the basis of the algorithm, program the chaos map into the micro-controller unit (MCU) or the micro-processor unit (MPU). Thirdly, convert the MCU or MPU output into the analogue signal via the digital-analogue conversion (DAC). Finally, linearize the analogue signal in order to suit the application.

4.4.2 Algorithm Design

According to Logistic equation (4.13), the system runs in chaos when the factor a and the initial value x_0 are chosen as follows: $a = 4x_0 = 0.3$. The key for the algorithm is how to convert x_{n+1} to the digital signal and the continuous waveform, such as the triangle, rectangle, sine and so on. Every discrete value is corresponding to the cycle of the wave. Denote the corresponding cycle is T_{n+1}, which is calculated as

$$T_{n+1} = \mathrm{N} \cdot (k \cdot (x_{n+1} - 0.5) + \mathrm{T_C}), \tag{4.16}$$

where $\mathrm{T_C}$ and N are set up as two constants and k is a adjusting factor. On the basis of Eq. (4.13), $x_n \in (0,1)$, hence, $(x_{n+1} - 0.5) \in (-0.5, +0.5)$ and T_{n+1} is the magnifying

result based on T_C with a left or right offset. That is $T_{n+1} \in (N(T_C - 0.5k), N(T_C + 0.5k))$. Once T_C, N and k are determined, the cycle T_{n+1} can be estimated. In another word, the wave can be expected through configuring T_C, N and k.
For a triangle wave, the algorithm flow chart is presented in Figure 4.6.

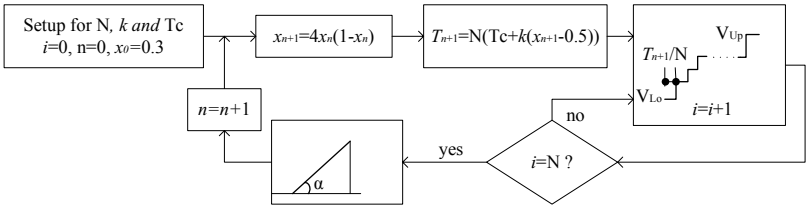


Figure 4.6: Algorithm flow chart of generating chaotic signal based on Logistic map

Assume the maximum and the minimum of the triangle wave as V_U and V_L respectively, as shown in Figure 4.7. From the algorithm, the (n+1)th wave undergoes N steps from the minimum V_L to the maximum V_U. Suppose that i, j, t are variables. There exists

$$v_t = V_L + (V_U - V_L)(t - \sum_{j=1}^{n} T_j), \sum_{j=1}^{n} T_j < t < \sum_{j=1}^{n+1} T_j, \tag{4.17}$$

where $t = \sum_{j=1}^{n} T_j + i\frac{T_{n+1}}{N}, i = 1, 2, ...N$, i is a counter that counts the running step, as shown in Figure 4.6.
The greater the value of N is, the smoother the waveform appears. Meanwhile, the time that every step holds also reflects the smoothness, which is determined by T_{n+1}/N.

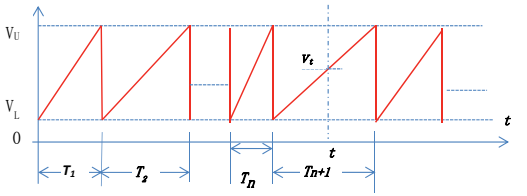


Figure 4.7: Triangle wave

Essentially, the algorithm converts the discrete variable of the chaos map to the changeable cycle of the wave. Hence, T_{n+1} is determined by x_{n+1} and the slope of the $(n+1)$th triangle

Table 4.3: The parameter configuation for the virtual oscillator

horizontal	trigger
source: trace	source: channel A
position: 250.00 mS	level: 1.00 V
S/Div: 25.00 mS	coupling: AC
	edge: Rising
	mode: Auto

wave is determined by T_{n+1}. Denote $\tan\alpha$ as the slope. It is calculated by

$$\tan\alpha = \frac{\mathrm{V_U} - \mathrm{V_L}}{T_{n+1}}. \tag{4.18}$$

Because x_{n+1} belongs to the chaos sequence, T_{n+1} varies chaotically and the triangle wave is chaotic.

4.4.3 Simulations and Experiments

a. Simulations

Normally, any MCU or MPU and DAC have their operating speed, which determines the maximum frequency of processed signals. In this premise, the speed of discrete status switching can be adjusted by the parameters like $\mathrm{T_C}$ and k according to Eq. (4.16).

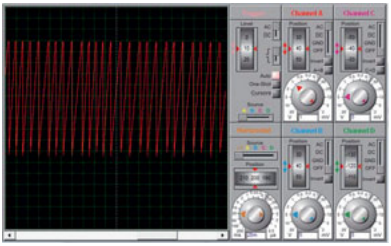
Simulation is implemented by the software Proteus 7.0. The micro-controller STC89C52RC and DAC1230LC are main components in the simulating schematic and the external oscillating frequency is 11.0592 MHz. The settings of virtual oscilloscope are followed in Table 4.3.

Figure 4.8 shows the output waves when $k = 10$ and $\mathrm{T_C}$ varies. Figure 4.8 (a), (b) and (c) are corresponding to the three different values of $\mathrm{T_C}$, 20, 10 and 5 respectively. According to the equation (4.16), while $\mathrm{T_C}$ is decreasing, T_{n+1} is decreasing, that is, the system is faster to convert x_{n+1} into chaotic analogue signal as demonstrated in Figure 4.8. On the contrary, the greater the $\mathrm{T_C}$, the slower the system completes the conversion.

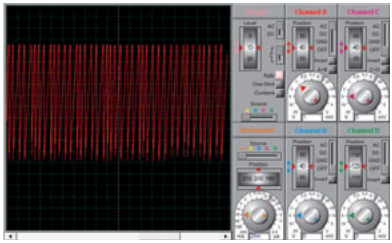
After the system having run for some time, it can be observed that the output waveform escapes from the chaos and appears periodic, as shown in Figure 4.9. The reason is that any MCU or MPU has a limited floating point arithmetic precision. The more times the variable iterates, the more information it loses. In the end, the output signal evolves to be periodic. The higher the floating point arithmetic precision is, the longer the variable keeps chaotic. However, the system will eventually run into the periodic status, so it is necessary to figure out the solution.

Basic thought of the solution is to reset and initialize the discrete map before entering the periodic status. One method is to unconditionally initialize the system in every fixed period of time. Another method is to reset the system only when the discrete series are detected to repeat cyclically, which means that $x_{n+1} = x_n$.

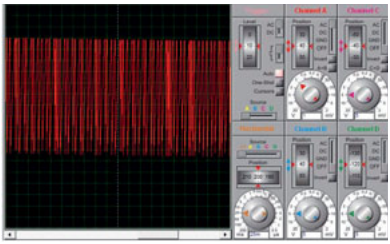
b. Experimental Results



(a) $T_C = 20$



(b) $T_C = 10$



(c) $T_C = 5$

Figure 4.8: DAC outputs with the different T_C

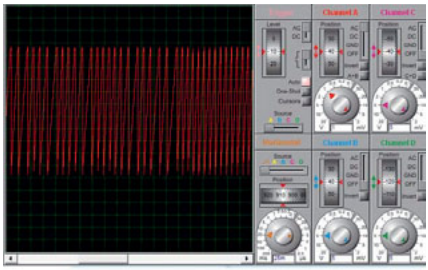


Figure 4.9: From chaos to periodic status

The hardware design is made on the basis of the schematic of the simulation. In order to facilitate, the MPU $STM32f10x\_dac$ with a module of DAC inside is used to replace the MCU STC89C52RC and DAC1230LC, as shown in Figure 4.10.
The algorithm of generating chaotic signal by Logistic map is accomplished in the microprocessor $STM32f10x\_dac$. After being converted by the DAC module, the processed signal undergoes the linearlization by two-stage $OP285GP$ amplifying circuit. Magnifying function is realized at the first stage, and the translation is completed at the second stage, so that the output chaotic signal has the reasonable range suitable for the application.
The experimental tests are demonstrated in Figure 4.11. Under the same value of k, T_C varies among 100, 25 and 3.6. Each sub-graph includes the time evolution and its Fast

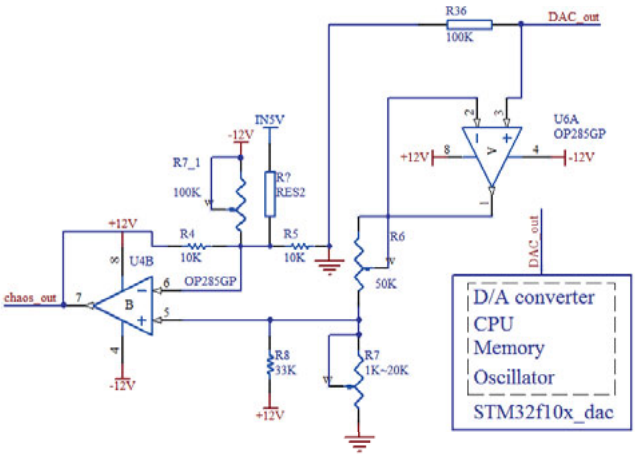


Figure 4.10: Schematic of the generating the chaotic signal

Fourier Transform (FFT).

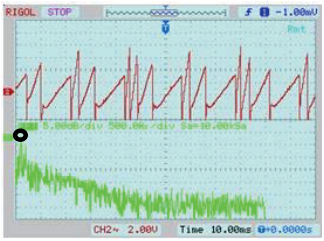
In Figure 4.11 (a), T_C=100, the time evolution is slow and the peak of FFT is located at 100 Hz, which demonstrates the main frequency component of the chaotic signal. In Figure 4.11 (b), T_C=25, the peak of FFT increases to 400 Hz. Figure 4.11 (c) shows the higher frequency of 2.8 kHz when T_C=3.6. The frequency of the FFT peak reflects the speed that the chaotic signal varies.

The tests are conducted on the output voltage of the power switch, and the sub-figures in Figure 4.12 show the output FFTs under the normal PWM control and the chaotic PWM control with the central frequency f_o equal to 100 Hz, 400 Hz, 2.8 kHz, respectively. With the normal control, the comparisons indicate that chaotic modulation suppresses EMI through reducing the amplitudes of the fundamental component and its harmonics components. What's more, the effectiveness of EMI suppression is improved along with the increasing value of central frequency f_o.

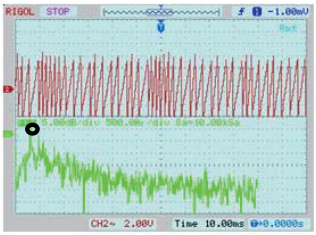
4.5 Summary

This chapter proves that the central frequency has an effect on the EMI suppression in switching converters under chaotic modulation. Simulation and experimental results have verified that it is optimal for reducing EMI with chaotic duty modulation when the central frequency of chaotic signal is close to one half of the switching frequency, which supplies a reference for the application of chaotic modulation.

Chaotic modulation is realized by two ways of the analogue circuit and the digital circuit. Chua's circuit and its improved circuits are commonly used to produce chaotic analogue signal. Although Chua's circuit is simple and mature, it is sensitive to the surrounding and device parameters, which leads to the variation between the chaos and multi-period status.



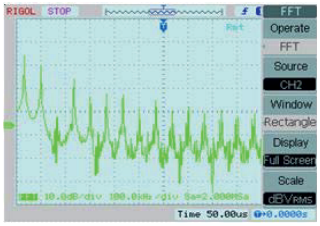
(a) $T_C = 100$



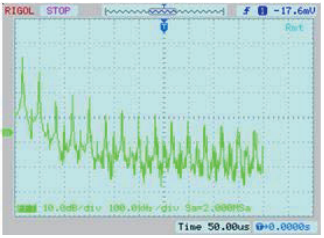
(b) $T_C = 25$

(c) $T_C = 3.6$

Figure 4.11: Chaotic signals and their spectra



(a) Normal PWM



(b) $f_o = 100$ Hz

(c) $f_o = 400$ Hz

(d) $f_o = 2.8$ kHz

Figure 4.12: FFT of the Switch Output Voltage under Normal PWM and Chaotic PWM

A chaotic digital signal is produced through programming the chaos map and burning the codes into MCU or MPU everlastingly, which has the shortcomings , such as the limited float precision and operating speed.

5 Realizing Chaotic Duty Modulation

5.1 Introduction

Spread spectrum modulation is categorized as four modes [30–32]: pulse width modulation with variable duty and fixed cycle (PWM), pulse position modulation with variable position of the pulse and fixed cycle (PPM), frequency modulation with variable duty (FMVD) and frequency modulation with fixed duty (FMFD). All the above modulations reduce the amplitudes of the fundamental component and its harmonics of the switching frequency [24]. Among the four modes, FMFD is the most effective spread spectrum [25], which is the most common mode used to spread the spectrum and suppress EMI in the switching converters [17, 21, 22]. However, FMFD is limited in applications because its varying frequency affects the circuit design and the power component selection.
The chaotic duty modulation keeps at a fixed frequency, which facilitates the action of the power components , such as power switch, high-frequency transformer and rectifier diode. In Chapter 3, the chaotic duty modulation was analyzed on spread spectrum used for suppressing EMI, and the implementation circuit for DC-DC buck converter was proposed for simulation verification. This chapter gives the method to implement the chaotic duty modulation in the half-bridge topology that is widely used in low-medium power output. The PC's power supply ATX2.0. is adopted to be the test bed. ATX2.0 has a typical integrated circuit (IC), TL494, which is a universal voltage-controlled PWM IC. Analogue and digital schemes of chaotic duty modulation are respectively designed on the basis of TL494. The simulation and experimental tests verify the effectiveness of the proposed schemes, and the comparisons of the results are made for them in the end.

5.2 Implementation of Chaotic Duty Modulation

In order to realize the chaotic PWM in half-bridge topology, the system includes the generation of the chaotic PWM, output sampling, PWM distribution and driver. In addition, the dead-time control is essential to avoid conducting two transistors of half-bridge at the same time. The schematic is shown in Figure 5.1, in which the sawtooth oscillator generates the wave with the fixed frequency.
The chaotic signal v_{ch} becomes v_{ref} after linearization and translation. There exists

$$v_{ref} = a_1 v_{ch} + b. \tag{5.1}$$

The displacement b is constant and a_1 is the scale coefficient. The amplifier output v_{con} is expressed as

$$v_{con} = k_A(v_{ref} - v_S) = k[(a_1 v_{ch} + b) - \eta v_O], \tag{5.2}$$

where k_A is the gain of the amplifier, η is the sampling coefficient. Denote V as the nominal output voltage. Hence, the practical output is $v_O = \mathrm{V} + \Delta v$ and the equation (5.2) is

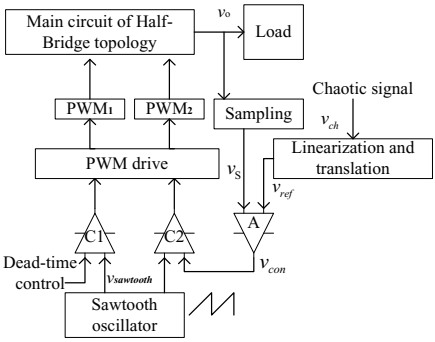


Figure 5.1: The schematic of half-bridge topology under chaotic modulation

described as

$$v_{con} = k_A(b - \eta \mathrm{V} + a_1 v_{ch} - \eta \Delta v) = k_A(b - \eta \mathrm{V}) + k_A(a_1 v_{ch} - \eta \Delta v). \tag{5.3}$$

PWM signal is obtained by comparing the amplifier output v_{con} and the sawtooth $v_{sawtooth}$ in the comparator C_2. Because $v_{sawtooth}$ possesses the fixed frequency and the amplitude, the duty of PWM is determined by v_{con}. In Eq. (5.3), v_{con} consists of the constant part $k_A(b - \eta \mathrm{V})$ and the chaotic variable part $k_A(a_1 v_{ch} - \alpha \Delta v)$.
The duty of chaotic modulation satisfies

$$d = \mathrm{D} + \Delta d, \tag{5.4}$$

where D is the duty of normal PWM and keeps constant. Chaotic duty modulation makes the duty of PWM fluctuate around D, and the variation is Δd. When Δd is chaos series, d is likewise. In Eq. (5.3), $k_A(b - \eta V)$ corresponds to D and $k_A(a_1 v_{ch} - \alpha \Delta v)$ to Δd, which implements the algorithm of chaotic duty.

5.3 Analogue Chaotic Duty Modulation

5.3.1 System and TL494

a. System Schematic
PC's power accessory is chosen as the test bed whose model is ATX 2.0. The power device possesses the following parameters.
nominal input voltage: 220 VAC
operating voltage range: 200∼240 V/3.5 A, 50 Hz
nominal output power: 200 W
multiple DC outputs: +3.3 V, +5 V, -5 V, +12 V, -12 V and +5 V standby.
The power system consists of many modules, as shown in Figure 5.2 [47]. The grid AC input is filtered and rectified to acquire the DC voltage 310 V, which provides the main

circuit with the source for power conversion. The main circuit includes half-bridge power conversion and the high-frequency transformer, as demonstrated in the dash-dotted line box of Figure 5.2. The output of high-frequency transformer proceeds to rectify and filter. Then, the multiple DC outputs are obtained in the low-pass filter network. PWM control module supervises the states of half-bridge transistors to conduct by turns with the suitable dead-time. There are some other modules like the auxiliary power, detection and protection. The external chaotic signal is connected to the PWM control module of ATX 2.0. The chaotic signal is produced by Chua's circuit and processed linearly, as shown in the dotted line box of Figure 5.2.

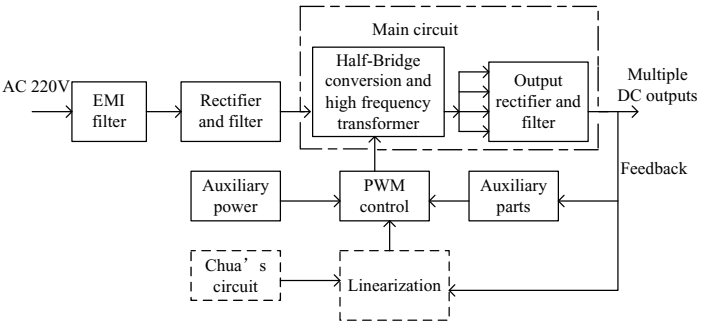


Figure 5.2: The PC's schematic under chaotic modulation

b. Chaotic Modulation Based on TL494

IC TL494 is a dedicated chip used for PWM control, which is a fixedCfrequency pulse width modulation control circuit. Its interior is shown in Figure 5.3 [48]. An internal linear sawtooth oscillator is frequencyCprogrammable by two external components, R_T and C_T. The oscillator frequency is determined by

$$f_O = \frac{1.1}{R_T C_T}. \tag{5.5}$$

The control signals are external inputs that are fed into the dead-time control (DTC) through the pin 4, the error amplifier inputs through the pins 1, 2, 15, 16, or the feedback input through the pin 3, as shown in Figure 5.3. Pulse width modulation is accomplished by comparing the positive sawtooth waveform across the capacitor C_T with either of non-inverting inputs of dead-time comparator and PWM comparator. The NOR gates, which drive output transistors T_1 and T_2, are enabled only when the flip-flop clock-input line, denoted by CK, is changed to low-level (logic 0). This happens only during that portion of time when the sawtooth voltage is greater than the control signals. Therefore, an increase

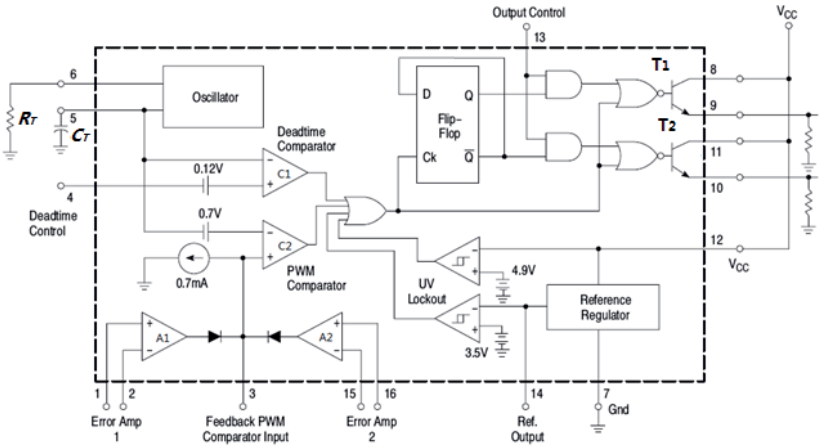


Figure 5.3: The block diagram of TL494

in control-signal amplitude causes a corresponding linear decrease of output pulse width. Assume that the output control at pin 13 keeps at high-level (logic 1).
Denote v_{ct} as the signal at the pin 5, v_{dead} as the input of the dead-time comparator, and v_{fdb} as the feedback input through the pin 3. An external chaotic signal v_{chao} is injected to TL494 through the pin 3, hence [48]

$$v_{fdb} = v_{chao}. \tag{5.6}$$

When $v_{ct} > v_{dead}$ and $v_{ct} > v_{chao} - 0.7$, there exists at the statue n

$$CK = 0, T_{1b} = \overline{Q_n}, T_{2b} = Q_n, \tag{5.7}$$

otherwise,

$$CK = 1, T_{1b} = 0, T_{2b} = 0, \tag{5.8}$$

where Q_n and $\overline{Q_n}$ represent the output of the flip-flop at the statue n, which are the opposite. If Q_n is at logic 1, $\overline{Q_n}$ is at logic 0. It is remarked that a change in chaotic signal amplitude causes a corresponding change of output pulse width, which accomplishes the chaotic duty modulation.

5.3.2 Design of Chaotic Signal Generator

This design is for generating the chaotic signal and connecting to the pin 3 of TL494, as shown in Figure 5.4. Module 1 is the chaotic signal generator, module 2 gets the feedback by output sampling, module 3 builds the reference voltage, and module 4 does amplifying. Module 1 is Chua's circuit, which is commonly adopted as the chaotic signal generator due to its maturity and simplicity. Nr is Chua's diode implemented by the active circuit. Chapter 4 has developed intensive study for Chua's circuit.

According to the TL494 specification [48], the electrical character of pin 3 is specified from 0.5 V to 3.5 V as the working voltage range. Accordingly, the output range of the amplifier is designed from 0.5 V to 3.5 V.

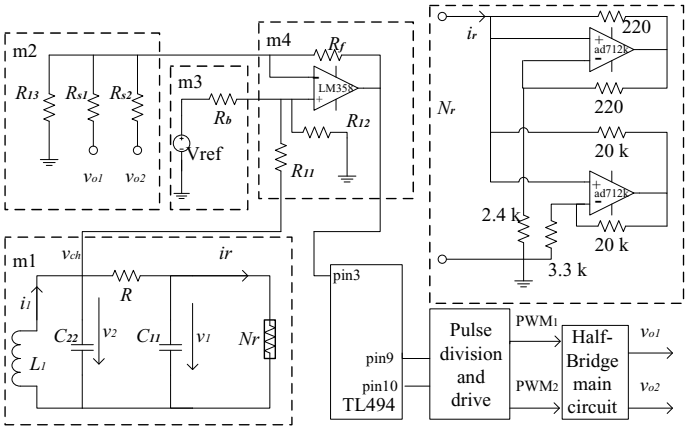


Figure 5.4: The chaotic PWM module

Combining module 2, 3, 4 together, based on the principle of the operating amplifier, the amplifier output is given by

$$v_{chao} = (1 + \frac{R_f}{R_{13}} + \frac{R_f}{R_{S1}} + \frac{R_f}{R_{S2}})(\frac{R_b R_{12} v_{ch} + R_{11} R_{12} \mathrm{V_{ref}}}{R_b R_{12} + R_{11} R_{12} + R_b R_{11}}) - \frac{R_f}{R_{S1}} v_{o1} - \frac{R_f}{R_{S2}} v_{o2}. \quad (5.9)$$

Let $1 + \frac{R_f}{R_{13}} + \frac{R_f}{R_{S1}} + \frac{R_f}{R_{S2}} = k'$, $\frac{R_b R_{12}}{R_b R_{12} + R_{11} R_{12} + R_b R_{11}} = a$ and $\frac{R_{11} R_{12}}{R_b R_{12} + R_{11} R_{12} + R_b R_{11}} = b$. When all the resistors, k', a and b keep constant, Eq. (5.9) is described by

$$v_{chao} = k'(a u_{ch} + b \mathrm{V_{ref}}) - \frac{R_f}{R_{S1}} v_{o1} - \frac{R_f}{R_{S2}} v_{o2}, \quad (5.10)$$

where $-\frac{R_f}{R_{S1}} v_{o1} - \frac{R_f}{R_{S2}} v_{o2}$ is the feedback of the system output and $\mathrm{V_{ref}}$ is the reference voltage. Basically, v_{chao} is in proportion to v_{ch} with the translation, so the variation trends of their waveforms are consistent.

5.3.3 Simulations and Experiments

a. Simulations

Assume that $R_T = 12\ \mathrm{k\Omega}$, $C_T = 1.5\ \mathrm{nF}$ and adopt the component parameters originating from the practical product ATX 2.0. The operating frequency of the IC internal oscillator

Table 5.1: The amplitudes of the fundamental of the switching frequency and its harmonics

Item	harmonic number	1	2	3	4	5	6	7	8
i_P (dB)	PWM	-8	4	-9	-15	-10	-9	-12	-20
	CPWM	-9	0	-19	-22	-18	-14	-25	-25
	decrement	1	4	10	7	8	5	13	5
i_{L+12} (dB)	PWM	-9	-2	-18	-18	-28	-27	-27	-32
	CPWM	-19	-10	-20	-20	-29	-38	-29	-32
	decrement	10	8	2	2	1	11	2	0
i_{L+5} (dB)	PWM	-10	-11	-30	-32	-41	-43	-47	-52
	CPWM	-20	-18	-34	-39	-48	-50	-50	-53
	decrement	10	7	4	7	7	7	3	1

is $f_{in} = 50$ kHz and the switching frequency f_s of the transistor is half of f_{in}. The parameters of Chua's circuit are chosen as $L_1 = 2.2$ mH, $C_{22} = 4.7$ nF, $C_{11} = 500$ pF, and $R = 1.75$ kΩ. The parameters of the operating amplifier and its peripheral components are $R_{11} = R_{12} = R_{13} = 10$ kΩ, $R_{s1} = 36$ kΩ, $R_{s2} = 90$ kΩ, and $R_f = 7$ kΩ. With these parameter settings, the simulations are conducted by Saber 7.0. Comparisons are made between the normal PWM control and the chaotic PWM control. Some typical power signals are chosen as the observed objects , such as

i_P, the current through the primary winding of the high frequency transformer.

i_{L+12}, the current through the output branch at +12 V.

i_{L+5}, the current through the output branch at +5 V.

Fast Fourier Transforms (FFTs) of the above signals are demonstrated in Figure 5.5. The EMI strength is commonly estimated according to the amplitudes of the fundamental of the switching frequency and its harmonics. Table 5.1 lists the amplitudes under the normal PWM control and the chaotic PWM control, respectively.

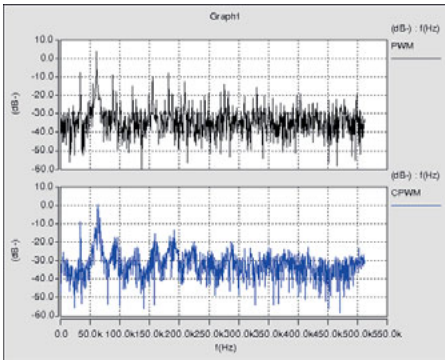
From Figure 5.5 and Table 5.1, the amplitudes of the fundamental of the switching frequency and its harmonics are reduced under the chaotic PWM, compared to those under the normal PWM control, indicating that the EMI is suppressed under the chaotic PWM.

b. Hardware Implementation and Experimental Tests

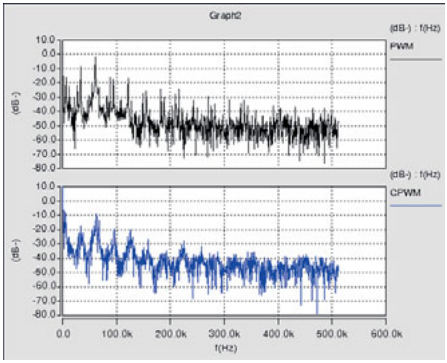
The hardware design and experiment are conducted to further verify the effectiveness of the chaotic PWM. Based on PC's power product ATX 2.0, an external part is designed for generating the chaotic signal and processing it, which makes the processed signal suitable for injecting TL494.

The improved Chua's circuit is proved to be easier to implement with hardware than the standard Chua's circuit. As shown in Figure 5.6, Chua's Diode N_r and the inductor L of Chua's oscillator respectively consist of two operating amplifiers which are powered by the outputs ±12 V of ATX 2.0. Copy the previous simulation circuit for N_r [49], whose parameters are $R_{d1} = 2.4$ kΩ, $R_{d2} = 3.3$ kΩ, $R_{d3} = R_{d4} = 220$ Ω, $R_{d5} = R_{d6} = 20$ kΩ.

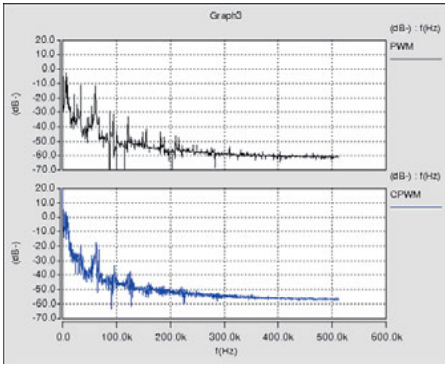
Refer to Rioden inductance circuit to build the inductor L [50], the peripheral component parameters are set as $R_1 = R_2 = R_3 = R_4 = 2$ kΩ, $C_1 = 10$ nF, $C_2 = 100$ nF, $C_3 = 4.7$ nF, and $R = 1.78$ kΩ. The hardware implementation and the experimental test are



(a) The current through the transformer



(b) The current through the output branch of +12 V



(c) The current through the output branch of +5 V

Figure 5.5: FFTs under the normal PWM (upper) and the chaotic PWM (lower)

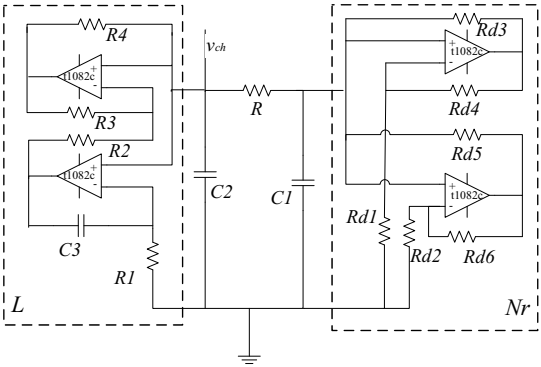


Figure 5.6: Improved Chua's circuit

demonstrated in Figure 5.7. Figure 5.8 shows the test result of the chaotic signal and the trajectory of $v_2 - v_1$ across the resistor R.

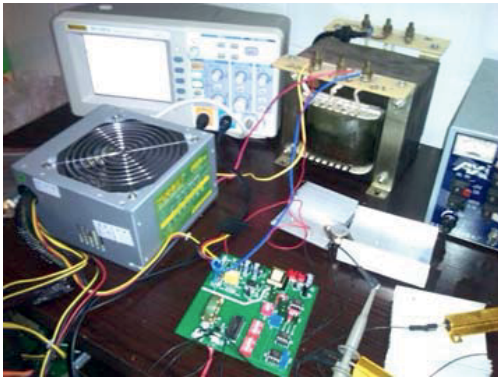
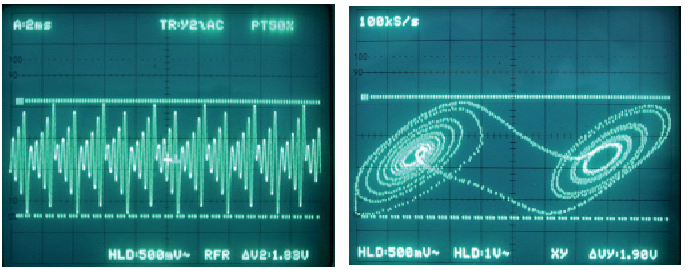


Figure 5.7: Experimental test

c. EMC Tests

The EMC tests are executed under the EMC standard EN55022 Class B Conducted QP and EN55022 Class B Conducted AV with the device ROHDE&SCHWARZ ESIB26 20 HZ-26.5 GHZ. The results of the EMI of the power supplier ATX 2.0 applying the conventional PWM and the chaos-based PWM are given in Figure 5.9, respectively, showing the



(a) The evolving wave of v_{ch} (b) The trajectory of $v_2 - v_1$

Figure 5.8: The experimental tests for the improved Chua's circuit

effectiveness of using the chaotic PWM for suppressing EMI. The following is the test configuration.

For Figure 5.9 (a) and (b), test range: 0.15 MHz-30 MHz, the bandwidth: 9 kHz, the step: 5 kHz.

For Figure 5.9 (c) and (d), test range: 0.15 MHz-2 MHz, the bandwidth: 200 Hz, the step: 100 Hz.

From the test results, the largest peak reaches to 55 dB under the normal PWM control, while it is reduced to 47 dB under the chaotic PWM control. Compared to those under the normal PWM control, the first peaks of EMI curve are flatten and the amplitudes of the fundamental component and its harmonics are reduced under the chaotic PWM control, which proves that EMI is suppressed under the chaotic modulation.

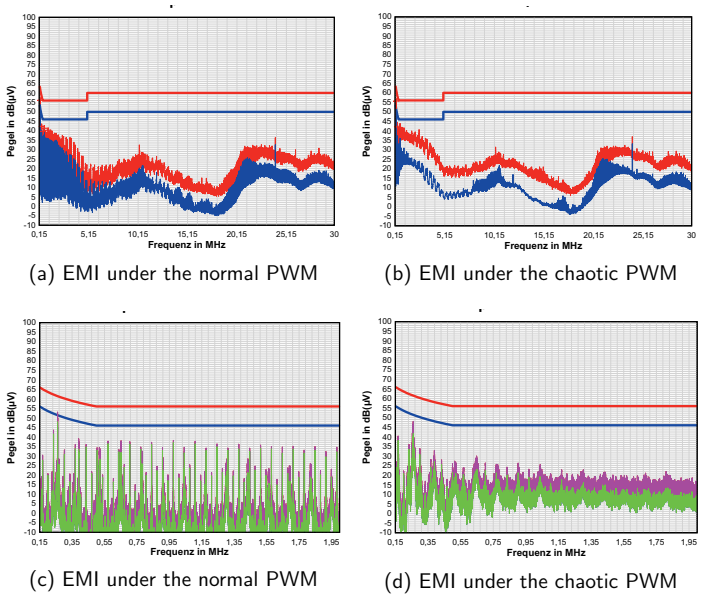
In Figure 5.10, the further observation is made for the EMI AV test, where the grey zone represents the normal PWM control and the black zone represents the chaotic PWM control. The comparison indicates that the amplitude variation range is less under the chaotic PWM than that under the normal PWM, and that the amplitude maximum is reduced by 5 dBμV.

5.4 Digital Chaotic Duty Modulation

5.4.1 Scheme Design

As shown in Figure 5.11, the design is made for half-bridge topology with digital chaotic modulation. The PWM module of the converter is injected by the external chaotic signal produced by the generator. The generator is composed of MPU, DAC and other modules, which are described in Chapter 4.

The application scheme is made and still applied on the power ATX2.0, which is demonstrated in Figure 5.12. STM32f10x_dac is used as MPU and DAC, whose oscillating frequency is 11.0592 MHz and MPU working frequency is 72 MHz. DAC output is processed linearly to suit the injecting pin of PWM module.



(a) EMI under the normal PWM

(b) EMI under the chaotic PWM

(c) EMI under the normal PWM

(d) EMI under the chaotic PWM

Figure 5.9: Conducted EMI tests

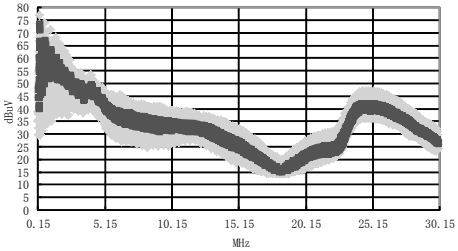


Figure 5.10: Test curves under the normal PWM (grey) and the chaotic PWM (black)

5.4.2 EMC Test

The EMC tests are exhibited in Figure 5.13. The blue curve is corresponding to QP test and the red curve to AV test. Figure 5.13 (a) and (b) are about the normal PWM and chaotic PWM, respectively. Table 5.2 lists the scanning values of the test curves, which illustrates that the amplitude redundancies of the first six peaks is greater under chaotic modulation than those under the normal PWM. The amplitude margin of the largest peak and the margin average of the first six peaks under the normal PWM are respective 14.03 dB and 23.51 dB, while those under the chaotic PWM are 16.30 dB and 27.23 dB.

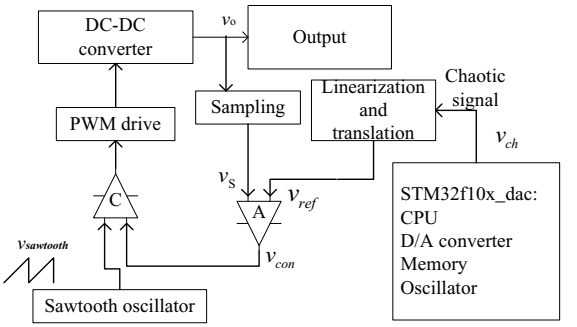


Figure 5.11: The diagram of voltage-controlled converter with digital chaotic modulation

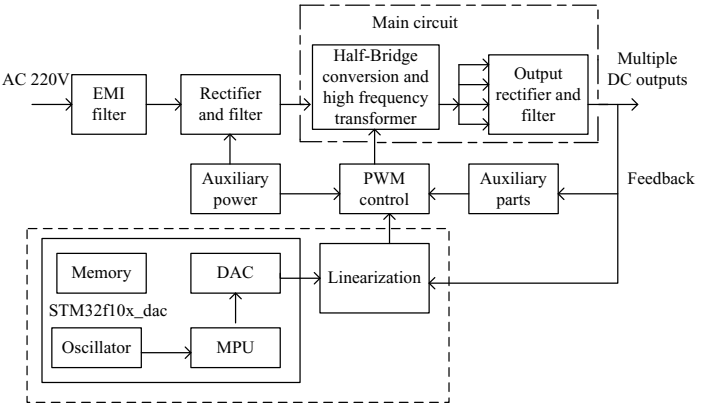
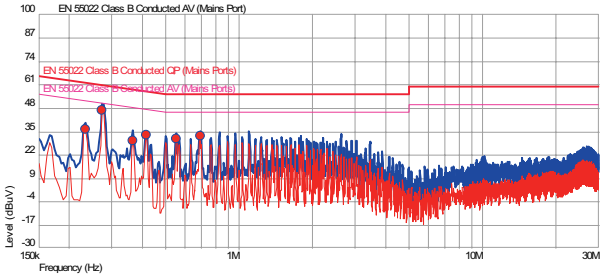


Figure 5.12: Digital chaotic modulation scheme for ATX 2.0

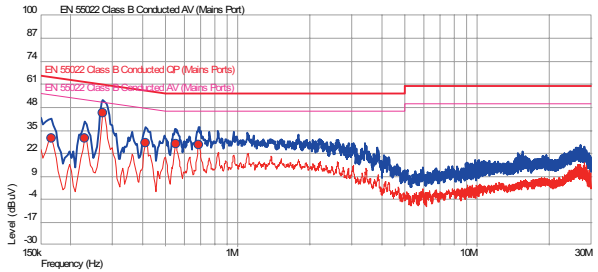
Therefore, the amplitudes of the fundamental component and its harmonics are reduced, that is, EMI is suppressed under chaotic modulation.

5.5 Summary

This chapter focuses on the application of chaotic duty modulation and develops the practical schemes on the basis of PC's power ATX 2.0. The suitable external chaotic signal is connected to PWM control module to accomplish the chaotic duty modulation. Because PWM IC is commonly used in the switching converter, the proposed scheme possesses the practical significance for the external chaotic signal injecting to the pre-existing PWM IC.



(a) The normal PWM control



(b) The chaotic PWM control

Figure 5.13: Conducted EMI tests

Table 5.2: Comparison of EMI AV tests (* margin of the largest peak)

Item	Frequency (Hz)	Level (dBuV)	Limit (dBuV)	Margin (dBuV)	Margin average
Chaotic PWM	166.0 k	30.75	65.16	34.41	27.23
	230.0 k	30.59	62.45	31.86	
	274.0 k	44.69	61.00	16.30*	
	410.0 k	27.64	57.65	30.01	
	550.0 k	27.43	56.00	28.57	
	686.0 k	26.61	56.00	29.39	
Normal PWM	234.0 k	36.13	62.31	26.17	23.51
	274.0 k	46.96	61.00	14.03*	
	366.0 k	30.10	58.59	28.49	
	414.0 k	33.20	57.57	24.37	
	550.0 k	31.24	56.00	24.76	
	690.0 k	32.79	56.00	23.21	

The analogue and digital schemes are respectively applied for the half-bridge power device to verify the EMI reduction effectiveness under chaotic modulation. The analogue scheme is simpler and maturer compared to the digital one. However, the component parameters in the analogue circuit are susceptive to the surroundings and a low accuracy. Digital scheme is realized by programming in micro-controller (MCU) or micro-processor (MPU), in which the algorithm codes keep unchanged in the surroundings. The central frequency can also be adjusted but limited, because the operating speeds are limited for MCU or MPU and DAC. High central frequency demands high-speed MCU or MPU, so there exists a compromise between the cost and the performance.

6 System Stability under Chaotic Duty Modulation

6.1 Introduction

The switching converter is a typical nonlinear control system because of the deployment of the nonlinear components , such as the power switch, the core inductance or transformer. Any disturbance possibly causes the deviation, which keeps the system away from the original state of equilibrium. Once the disturbance disappears, the system gets back to a state of equilibrium, which is named as the stability of the control system [43].
According to the classical control theory, the stability analysis of the switching converter is normally based on its kinetics models. As one of the kinetics models, the average model (AM) is categorized as the state space model (SSM) [51] and the circuit average model (CAM) [52]. Hong Li applied SSM to analyze the stability of boost converter with chaotic frequency modulation [53], and CaliskanV used CAM to verify the stability of the soft-switch converter [54]. Because CAM focuses on the switching character, such as conducting resistors of transistors and diodes, the equivalent circuit model is of high precision. The steps of applying CAM for stability analysis are as follows.
(1) According to the basic relations among the voltage, the current and the power of each component, the average large signal model (ALSM) is established through equivalently averaging the system variables during a switching period.
(2) Impose the disturbance on ALSM and construct the direct current model (DCM) and the small signal circuit model (SSCM).
(3) According to SSCM, the closed-loop transfer function is built via Laplace Transform.
(4) Analyze the stability on the basis of the transfer function.
The switching converter includes the power conversion, feedback, sampling, compensation control and PWM control. For each module, its transfer function is obtained from SSCM, based on which the system transfer function comes into being. Then, the phase redundancy and the gain redundancy can be obtained by Potter diagram or direct calculation of the transfer function, by which the system stability can be estimated. This chapter is to explore how to maintain the system stability in a switching converter under chaotic modulation.

6.2 Circuit Average Model of a Half-Bridge Converter

6.2.1 Circuit Description

Figure 6.1 shows a half-bridge topology converter, which includes the nonlinear transformer with the leak inductance and equivalent serial resistor. Assume that the current through the primary winding of the transformer rises linearly during the “ON” state. Output inductor keeps continuous current and two transistors (power switches) never operate in shoot-through.

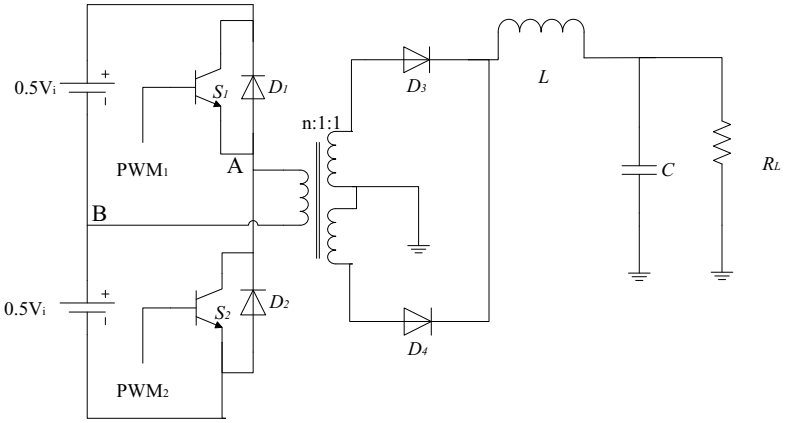


Figure 6.1: Half-bridge topology converter

Some hypothetical conditions are made for modelling the half-bridge converter [55].
(1) Parameters of two transistors are identical and those of two diodes are also identical.
(2) The output capacitor of the transistor and the capacitor of the diode are neglected. All the switching powers are regarded as zero.
(3) For the transistor, its equivalent resistor is linear during "ON" state, but infinite during "OFF" state.
(4) For the diode, it is regarded as the combination of a linear power and a linear resistor during "ON" state, but the infinite resistor during "OFF" state.
(5) The passive component is linear and time-invariance.
(6) The inductor current keeps constant during the switching process, which means that the current instantaneous value equals the DC component [56].
(7) The output impendence of the input voltage power is regarded as zero.
Simulated by the software Saber 7.0, the main working waves are demonstrated in Figure 6.2. Denote the duty of PWM_1 or PWM_2 as D and the cycle as T. Thus, $t_1 = \mathrm{DT}$, $t_2 = \frac{\mathrm{T}}{2}$, $t_3 = \frac{\mathrm{T}}{2} + \mathrm{DT}$ and $t_4 = \mathrm{T}$.
At the initial time, the switch S_1 runs into the conducting state under the positive pulse of PWM_1. The conducting current can't change instantly because of the inductance of the transformer. The current through the collector of the switch keeps rising linearly (The rising slope is $\frac{0.5\mathrm{V_i}}{L_P+L_{KP}}$, $\mathrm{V_i}$ is the input, L_P is the primary inductance of the transformer and L_{KP} is the primary leakage inductance). There exists $\mathrm{U_{AB}}$ equal to $\frac{1}{2}\mathrm{V_i}$ while assuming the terminal "A" the positive potential. At the same time, the currents through the switch and the primary winding of the transformer feed the load current and the magnetizing current of the transformer.
At the time t_1, the positive pulse of PWM_1 comes to an end, as well as the switch S_1 runs into the close state. The current continues flowing to the starting terminal of the primary

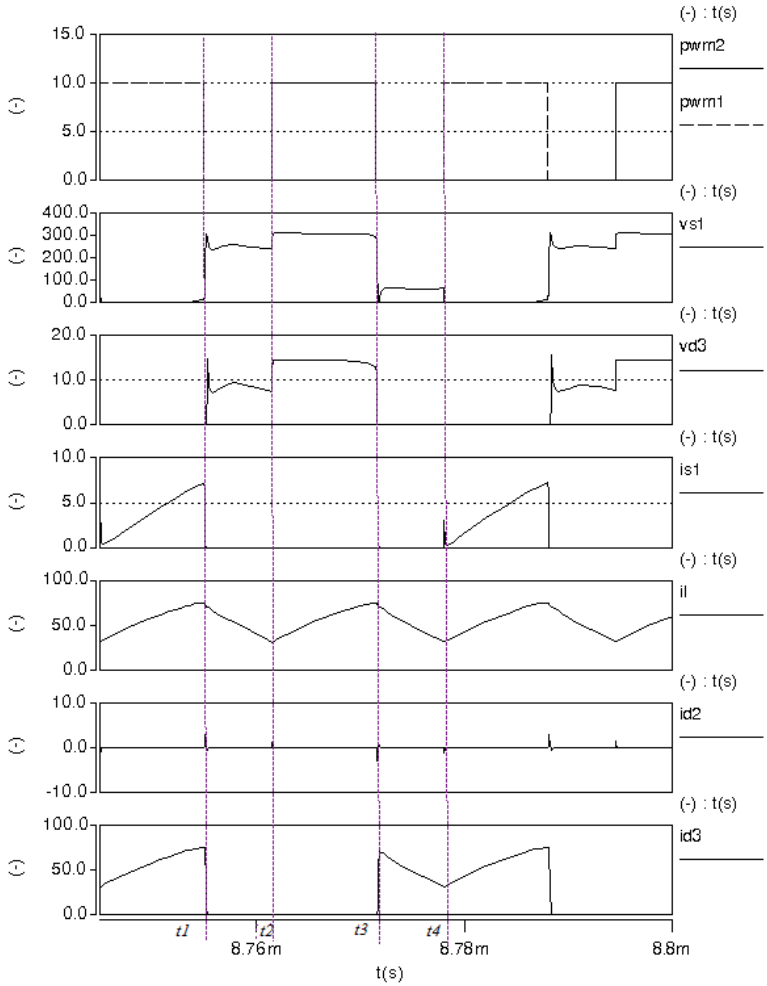


Figure 6.2: The working waves of the symmetric half-bridge converter

winding because of the inductance of the transformer, but the potential of the terminal "A" turns into the opposite and U_{AB} becomes $-\frac{1}{2}V_i$. Thus, the diode D_2 runs into the conducting state instantly, then it runs into the close state rapidly. Meanwhile, the current through the primary winding falls to zero quickly. Because U_{AB} is slightly less than $\frac{1}{2}V_i$, it maintains the continuous current through the secondary winding. To the time t_2, the positive pulse of PWM_2 arrives.

At the time t_2, the switch S_2 begins to conduct and the current through its collector rises

linearly (The rising slope is $\frac{0.5\mathrm{V_i}}{L_P+L_{KP}}$). The potential of the terminal "A" is negative, and $\mathrm{U_{AB}}$ is equal to $-\frac{1}{2}\mathrm{V_i}$.

At the time t_3, the switch S_2 closes. The potential of the terminal "A" changes into the positive, and $\mathrm{U_{AB}}$ becomes $\frac{1}{2}\mathrm{V_i}$. The diode D_1 conducts instantly, then close instantly. Meanwhile, the current through the primary winding falls to zero rapidly. Because $\mathrm{U_{AB}}$ is slightly less than $\frac{1}{2}\mathrm{V_i}$, it maintains the continuous current through the secondary winding.

The time t_4 is the end of the whole cycle and the beginning of the next new cycle.

For the output loop of the transformer, the Diode D_3 conducts while the switch S_1 is "ON" and the current through D_3 keeps the direction the same as the current through the primary winding. Once S_1 is "OFF", D_2 conducts. Meanwhile, the voltage across the primary winding turns into the negative, D_3 closes and D_4 conducts. When D_2 turns into closing, the negative voltage across the primary winding still exists. Thus, D_4 continues to conduct with a falling current.

Once the switch S_2 is "ON", D_4 continues to conduct with a rising current until S_2 changes into "OFF". D_1 conducts while S_2 is "OFF". Therefore, the voltage across the primary winding becomes positive, D_4 closes and D_3 conducts. When D_1 turns into closing, the positive voltage across the primary winding still exists. Thus, D_3 continues to conduct with a falling current until the next new cycle comes.

The cycle of PWM_1 or PWM_2 has been denoted as T before, thus, the switching frequency is $f_s = \frac{1}{\mathrm{T}}$. Denote the "ON" time slot as t_{on} and the "OFF" time slot as t_{off}. So, $\mathrm{T} = t_{on} + t_{off}$. For the symmetric half-bridge topology, the duty of each switch PWM satisfies the expression $\mathrm{D} = \frac{t_{on}}{\mathrm{T}} \leq 0.5$.

Figure 6.3 is the equivalent circuit with the conducting loss and the leakage inductance, where

R_{on} the conducting resistor of power switch

R_{tp} the resistor of the primary winding

R_{ts} the resistor of the secondary winding

$\mathrm{V_F}$ the forward voltage drop of the diode

R_F the forward resistor of the diode

R_{leqr} the equivalent serial resistor of the inductor L

R_{ceqr} the equivalent serial resistor of the capacitor C.

Denote i_L and I_L as the current instantaneous value and the DC component, respectively. According to the previous assumption, there exists i_L=I_L. i_{S_1}, i_{S_2} and I_{S_1}, I_{S_2} are the current instantaneous values and the DC components of the switches S_1 and S_2. i_{D_3}, i_{D_4} and I_{D_3}, I_{D_4} are the current instantaneous values and the DC components of the diodes D_3, D_4.

6.2.2 Large Signal Model

a. The Equivalent Average Resistor

When the diode D_3 conducts, the current through it is expressed as

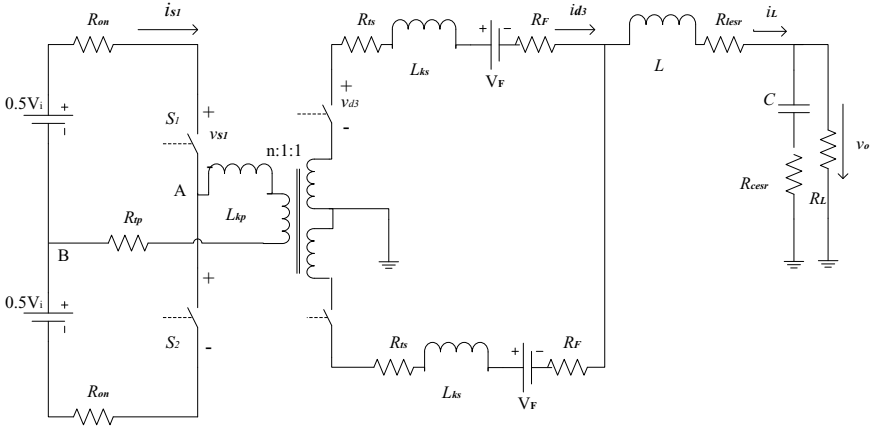


Figure 6.3: The equivalent circuit with parasitic elements

$$i_{D3} = \begin{cases} i_L, 0 \leq t < t_1, \\ 0, t_1 \leq t < t_3, \\ i_L, t_3 \leq t < t_4, \end{cases} \tag{6.1}$$

where $t_1 = \mathrm{DT}$, $t_3 = \frac{\mathrm{T}}{2} + \mathrm{DT}$, $t_4 = \mathrm{T}$. Hence,

$$\begin{aligned} \int_0^{\mathrm{T}} i_{D_3} dt &= \int_0^{t_1} i_{D_3} dt + \int_{t_1}^{t_3} i_{D_3} dt + \int_{t_3}^{t_4} i_{D_3} dt \\ &= \int_0^{\mathrm{DT}} i_{D_3} dt + \int_{\mathrm{DT}}^{\frac{\mathrm{T}}{2}+\mathrm{DT}} i_{D_3} dt + \int_{\frac{\mathrm{T}}{2}+\mathrm{DT}}^{\mathrm{T}} i_{D3} dt \\ &= \int_0^{\mathrm{DT}} i_L dt + \int_{\frac{\mathrm{T}}{2}+\mathrm{DT}}^{\mathrm{T}} i_L dt \\ &= \int_0^{\mathrm{DT}} i_L dt + \int_{\mathrm{DT}}^{\frac{\mathrm{T}}{2}} i_L dt \\ &= \frac{1}{2} \int_0^{\mathrm{T}} i_L dt. \end{aligned} \tag{6.2}$$

According to the previous equation, there exists

$$i_{D_3} = \frac{i_L}{2}. \tag{6.3}$$

On the basis of the above-mentioned assumption, $I_L = i_L$. I_S is the average current through the switching branch, V_D and V_S are the average voltages of the ideal diode and the ideal switch, respectively. During a cycle with the duty D, the current i_{S_1} through the switch S_1 goes through two different cases. When $0 \leq t < \mathrm{DT}$, $i_{S_1} \neq 0$ and $i_{S_1} \approx \frac{1}{n} I_L$. When $\mathrm{DT} \leq t < \mathrm{T}$, $i_{S_1} = 0$. Therefore,

$$\int_0^{\mathrm{T}} i_{S_1} dt = \int_0^{\mathrm{DT}} i_{S_1} dt + \int_{\mathrm{DT}}^{\mathrm{T}} i_{S_1} dt = \int_0^{\mathrm{DT}} i_{S_1} dt \approx \frac{1}{n} \int_0^{\mathrm{DT}} I_L dt = \frac{1}{n} \int_0^{\mathrm{DT}} i_{D_3} dt. \tag{6.4}$$

Because $\int_0^{\mathrm{DT}} i_{D_3} dt = \frac{\mathrm{DT}}{\frac{\mathrm{T}}{2}} \int_0^{\mathrm{T}} i_{D_3} dt$, there

$$\int_0^{\mathrm{T}} i_{S_1} dt \approx \frac{1}{n} \int_0^{\mathrm{DT}} i_{D_3} dt = \frac{2\mathrm{D}}{n} \int_0^{\mathrm{T}} i_{D_3} dt. \tag{6.5}$$

Further, the following expressions are obtained.

$$I_{S_1} = \frac{2\mathrm{D}}{n} I_{D_3}, i_{S_1} = \frac{2\mathrm{D}}{n} i_{D_3}. \tag{6.6}$$

For the symmetric half-bridge topology, $I_{D_4} = I_{D_3}$. On the basis of Kirchhoff's current law [57], $I_L = I_{D_3} + I_{D_4}$. There exists

$$I_{D_3} = \frac{I_L}{2}. \tag{6.7}$$

The equations (6.6) and (6.7) are the DC components of the transistor switch and the diode, respectively.

According to the operating principle, the output voltage v_{S_1} of the switch evolves in accordance with the following conditions.

When $0 \leq t < \mathrm{DT}$, $v_{S_1} = 0$.

When $\mathrm{DT} \leq t < \frac{\mathrm{T}}{2}$, $v_{S_1} \approx \mathrm{V_i}$.

When $\frac{\mathrm{T}}{2} \leq t < \frac{\mathrm{T}}{2} + \mathrm{DT}$, $v_{S_1} = \mathrm{V_i}$.

When $\frac{\mathrm{T}}{2} + \mathrm{DT} \leq t < \mathrm{T}$, $v_{S_1} \approx 0$.

The DC component V_{S_1} of the switch voltage v_{S_1} is

$$
\begin{aligned}
V_{S_1} &= \frac{1}{\mathrm{T}}\Big[\int_{0}^{\mathrm{DT}} v_{S_1}dt + \int_{\mathrm{DT}}^{0.5\mathrm{T}} v_{S_1}dt + \int_{0.5\mathrm{T}}^{0.5\mathrm{T+DT}} v_{S_1}dt + \int_{0.5\mathrm{T+DT}}^{\mathrm{T}} v_{S_1}dt\Big] \\
&\approx \frac{1}{T}\Big[\int_{0}^{\mathrm{DT}} 0dt + \int_{\mathrm{DT}}^{0.5\mathrm{T}} \mathrm{V_i}dt + \int_{0.5\mathrm{T}}^{0.5\mathrm{T+DT}} \mathrm{V_i}dt + \int_{0.5\mathrm{T+DT}}^{\mathrm{T}} 0dt\Big] \\
&= \frac{1}{\mathrm{T}}\Big[\int_{\mathrm{DT}}^{0.5\mathrm{T}} \mathrm{V_i}dt + \int_{0.5\mathrm{T}}^{0.5\mathrm{T+DT}} \mathrm{V_i}dt\Big] \\
&= \mathrm{V_i}(0.5-\mathrm{D}) + \mathrm{V_i D} = \frac{\mathrm{V_i}}{2}.
\end{aligned} \tag{6.8}
$$

The diode voltage would be equal to the switch voltage if the duty D is great enough. According to the references [55, 58], there exists

$$V_{D_3} = \frac{2\mathrm{D}V_{S_1}}{n} = \frac{2\mathrm{DV_i}}{n}. \tag{6.9}$$

Because S_1 and S_2 are identical and work symmetrically in turn, D_3 and D_4 are likewise, the following expressions are obtained.

$$I_D = I_{D_3} = I_{D_4} = \frac{I_L}{2}. \tag{6.10}$$

$$I_S = I_{S_1} = I_{S_2} = \frac{2\mathrm{D}}{n} I_{D_3} = \frac{\mathrm{D}}{n} I_L. \tag{6.11}$$

$$V_S = V_{S_1} = V_{S_2} = \frac{\mathrm{V_i}}{2}. \tag{6.12}$$

$$V_D = V_{D_3} = V_{D_4} = \frac{2\mathrm{D}V_{S_1}}{n} = \frac{\mathrm{DV_i}}{n}. \tag{6.13}$$

When $0 \leq t < \mathrm{DT}$, $i_S \neq 0$ and $i_S \approx \frac{1}{n} I_L$. When $\mathrm{DT} \leq t < \mathrm{T}$, $i_S = 0$. From the expression $I_S = \frac{\mathrm{D}}{n} I_L$, it is obtained that $I_L = \frac{n}{\mathrm{D}} I_S$. On the basis of the definition of the root-mean-square (RMS) [57], the switch current RMS is

$$
\begin{aligned}
I_{Srms} &= \sqrt{\frac{1}{\mathrm{T}}\int_{0}^{\mathrm{T}} i_s^2 dt} = \sqrt{\frac{1}{\mathrm{T}}\int_{0}^{\mathrm{DT}} i_s^2 dt} \approx \sqrt{\frac{1}{\mathrm{T}}\int_{0}^{\mathrm{DT}} (\frac{I_L}{n})^2 dt} \\
&= \sqrt{\frac{1}{\mathrm{T}}(\frac{I_L}{n})^2 \mathrm{DT}} = \sqrt{(\frac{I_L}{n})^2 \mathrm{D}} = \sqrt{(\frac{I_s n}{\mathrm{D}n})^2 \mathrm{D}} = \frac{I_s}{\sqrt{\mathrm{D}}}.
\end{aligned} \tag{6.14}
$$

From the equation (6.3), the diode current RMS is

$$I_{Drms} = \sqrt{\frac{1}{\mathrm{T}}\int_0^{\mathrm{T}} i_D^2 dt} = \sqrt{\frac{1}{2\mathrm{T}}\int_0^{\mathrm{T}} i_L^2 dt} = \frac{\sqrt{2}}{2} I_{Lrms} = \frac{\sqrt{2}}{2} I_L = \sqrt{2} I_D \approx \frac{n\sqrt{2} I_S}{2\mathrm{D}}. \quad (6.15)$$

The total conducting loss of R_{on} and R_{tp} is

$$P_1 = (R_{on} + R_{tp}) I_{Srms}^2 = (R_{on} + R_{tp}) \Big(\frac{I_S}{\sqrt{\mathrm{D}}}\Big)^2 = \frac{R_{on} + R_{tp}}{\mathrm{D}} I_S^2. \quad (6.16)$$

The magnetic energy of the primary leakage is

$$W_{LKP} = \frac{1}{2} L_{KP} I_{Srms}^2 = \frac{1}{2} L_{KP} \Big(\frac{I_S}{\sqrt{\mathrm{D}}}\Big)^2 = \frac{1}{2} \frac{L_{KP}}{\mathrm{D}} I_S^2. \quad (6.17)$$

The magnetic energy of the secondary leakage is

$$W_{LKS} = \frac{1}{2} L_{KS} I_{Drms}^2 = \frac{1}{2} L_{KS} \Big(\sqrt{2} I_D\Big)^2 = \frac{1}{2} (2L_{KS}) I_D^2. \quad (6.18)$$

The power loss of R_F and R_{ts} is totally

$$P_2 = (R_F + R_{ts}) I_{Drms}^2 = 2(R_F + R_{ts}) I_D^2. \quad (6.19)$$

The power consumption of the forward voltage drop $\mathrm{V_F}$ is

$$P_{VF} = \mathrm{V_F} I_D = \frac{\mathrm{V_F} I_L}{2}. \quad (6.20)$$

b. Large Signal Model

From Eq. (6.16), the equivalent average resistor of the power switch branch is $\frac{R_{on}+R_{tp}}{\mathrm{D}}$.
From Eq. (6.17), the equivalent average leakage of the power switch branch is $\frac{L_{KP}}{\mathrm{D}}$.
From Eq. (6.18), the equivalent average leakage of the output diode branch is $2L_{KS}$.
From Eq. (6.19), the equivalent average resistor of the output diode branch is $2(R_F + R_{ts})$.
Considering the above equivalent average components, ALSM is built as shown in Figure 6.4. From Eqs. (6.11) and (6.13), the average current through the switch branch and the average voltage across the ideal output diode are respectively

$$I_S = \frac{\mathrm{D}}{n} I_L, V_D = \frac{2\mathrm{D}}{n} V_S = \frac{\mathrm{D}}{n} \mathrm{V_i}. \quad (6.21)$$

In terms of the principle of energy conservation, all the conducting resistance is converted into the loss resistance of the inductor, therefore, the model shown in Figure 6.4 is simplified and demonstrated in Figure 6.5. In the light of the calculating the resistance loss and the inductance magnetic energy, the following expressions are obtained.

$$P_1 = \frac{R_{on} + R_{tp}}{\mathrm{D}} I_S^2 = \frac{R_{on} + R_{tp}}{\mathrm{D}} \Big(\frac{\mathrm{D}}{n} I_L\Big)^2 = \frac{\mathrm{D}(R_{on} + R_{tp})}{n^2} I_L^2, \quad (6.22)$$

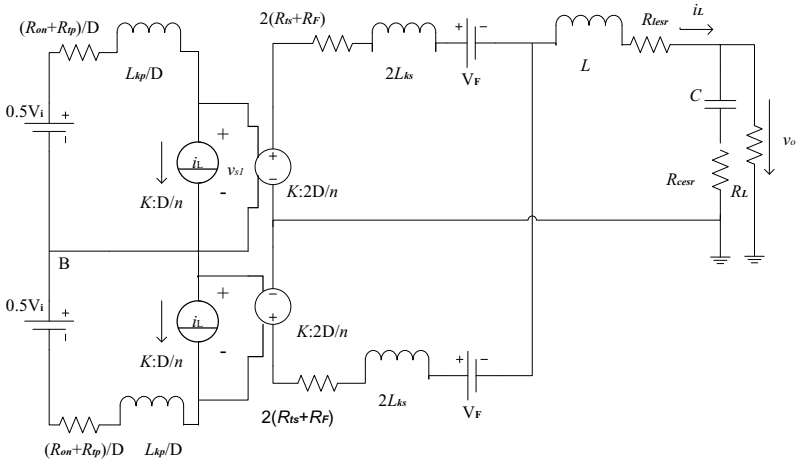


Figure 6.4: ALSM of half-bridge circuit with the original average parasitical components

$$P_2 = 2(R_F + R_{ts})I_D^2 = \frac{1}{2}(R_F + R_{ts})I_L^2, \tag{6.23}$$

$$P_{VF} = \mathrm{V_F} I_D = \frac{\mathrm{V_F} I_L}{2}, \tag{6.24}$$

$$W_{LKP} = \frac{1}{2}\frac{L_{KP}}{D} I_S^2 = \frac{1}{2}\frac{L_{KP}}{\mathrm{D}}\left(\frac{\mathrm{D}}{n} I_L\right)^2 = \frac{1}{2}\frac{\mathrm{D} L_{KP}}{n^2} I_L^2, \tag{6.25}$$

and

$$W_{LKS} = \frac{1}{2}\Big(2L_{KS}\Big) I_D^2 = \frac{1}{2}\Big(2L_{KS}\Big)(\frac{I_L}{2})^2 = \frac{1}{2}\Big(\frac{1}{2}L_{KS}\Big) I_L^2. \tag{6.26}$$

Hence, take the output inductor branch as the destination. The conversions are made for the following.

The equivalent average resistor of the switch branch $\frac{R_{on}+R_{tp}}{\mathrm{D}}$ is converted into $\frac{\mathrm{D}(R_{on}+R_{tp})}{n^2}$. The equivalent average resistor of the diode branch $2(R_F + R_{ts})$ is converted into $\frac{1}{2}(R_F + R_{ts})$, and the equivalent average voltage is $\frac{\mathrm{V_F}}{2}$.

The primary leakage is converted into $\frac{\mathrm{D}L_{KP})}{n^2}$ and the secondary leakage is converted into $\frac{1}{2}L_{KS}$, so the equivalent average inductor is

$$L_{eq} = \frac{2\mathrm{D}L_{KP}}{n^2} + L_{KS} + L. \tag{6.27}$$

The equivalent average resistor R_{eq} serial to L_{eq} is

$$R_{eq} = \frac{2\mathrm{D}(R_{on} + R_{tp})}{n^2} + R_F + R_{ts} + R_{lesr}. \tag{6.28}$$

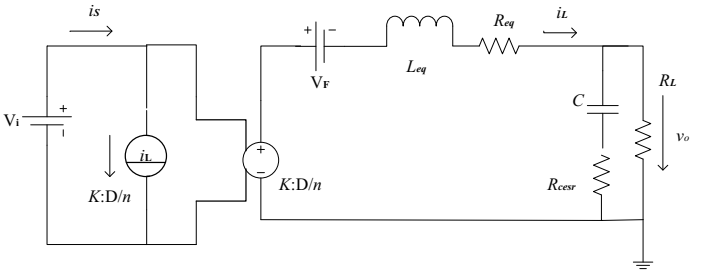


Figure 6.5: ALSM of half-bridge circuit with the average parasitical components converted to the inductor branch

Based on ALSM, the disturbance is exerted on the input and output. DC model is built under three hypotheses, such as open circuit for capacitors, short circuit for inductors and zero disturbance. Some parameters can be calculated on direct current model (DCM). If the disturbance is focused on ALSM without considering the steady components like the constant-current or constant-voltage source, SSCM is established by linearizing the small signal near the steady state operating point.

6.2.3 Direct Current Model and Small Signal Model

Exert the disturbance on the input and output in Figure 6.5 [55, 58]. Assume the input disturbance as Δu_i and the output disturbance as Δu_o. Each instantaneous value is the sum of the steady component and the disturbance, that is $v_i = \mathrm{V_i} + \Delta v v_o = V_o + \Delta v, d = \mathrm{D} + \Delta d$, $i_L = I_L + \Delta i_L$.
From the equation (6.11), there exists

$$i_S = I_S + \Delta I_S = \frac{\mathrm{D} + \Delta d}{n}(I_L + \Delta i_L) = \frac{\mathrm{D}}{n} I_L + \frac{\mathrm{D}}{n}\Delta i_L + \frac{I_L}{n}\Delta d + \frac{\Delta i_L}{n}\Delta d, \tag{6.29}$$

$$v_D = V_D + \Delta v_D = \frac{\mathrm{D} + \Delta d}{n}(V_i + \Delta v_i) = \frac{\mathrm{D}}{n} V_i + \frac{\mathrm{D}}{n}\Delta v_i + \frac{\mathrm{V_i}}{n}\Delta d + \frac{\Delta v_i}{n}\Delta d. \tag{6.30}$$

a. Direct Current Model
When analyzing the steady state of the circuit, the inductor L_{eq} is regarded as being short-circuit, the capacitor C is considered as being open-circuit and the disturbance is supposed zero. According to Eqs. (6.29) and (6.30), DC model is built for the continuous working mode, which is shown in Figure 6.6.
On the basis of this DC model, some steady state components can be calculated like V_o and I_L.

$$V_o = \frac{\frac{\mathrm{DV_i}}{n} - \mathrm{V_F}}{1 + \frac{R_{eq}}{R_{load}}}, \tag{6.31}$$

$$I_L = \frac{V_o}{R_{load}}. \tag{6.32}$$

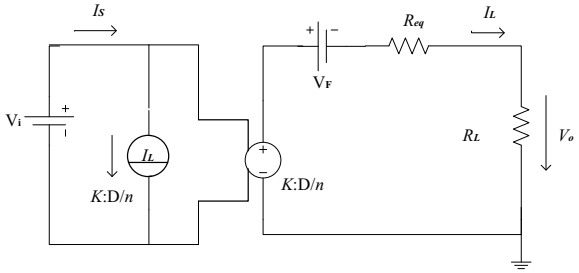


Figure 6.6: DC model of half-bridge converter

b. Small Signal Circuit Model

The steady state components are supposed to be zero while analyzing the small signal. Now, $\frac{\Delta d}{\mathrm{D}} \ll 1$, $\frac{\Delta i_L}{I_L} \ll 1 \frac{\Delta v_i}{\mathrm{V_i}} \ll 1$, so $\frac{\Delta i_L}{n}\Delta d$ and $\frac{\Delta v_i}{n}\Delta d$ are neglected. Then Eqs. (6.29) and (6.30) are described as

$$\Delta i_S = \frac{\Delta d}{n} I_L + \frac{\mathrm{D}}{n}\Delta i_L, \tag{6.33}$$

$$\Delta v_D = \frac{\Delta d}{n} V_i + \frac{\mathrm{D}}{n}\Delta v_i. \tag{6.34}$$

The equivalent circuit is shown in Figure 6.7. SSCM is the basis for gaining the transfer function and analyzing system stability.

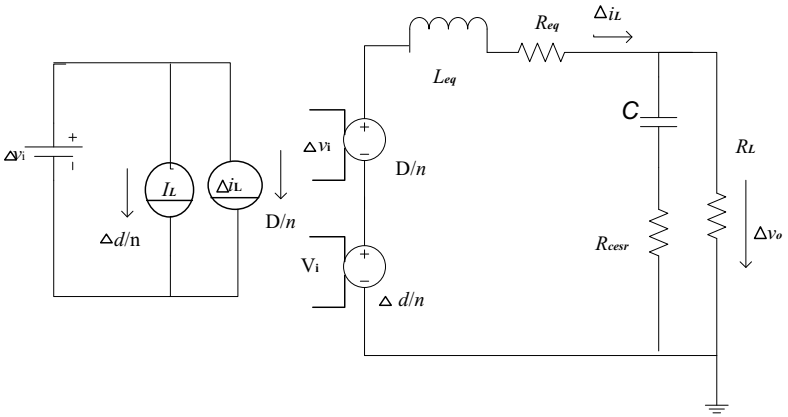


Figure 6.7: The small signal circuit model of half-bridge topology

6.3 Stability

A typical switching converter consists of power conversion, PWM control, compensating control and error feedback. Here, take the voltage-controlled PWM IC labelled TL494 as the instance. For the chaotic duty modulation, the external disturbance is injected to the compensating control, which functions the sum operation between the chaotic signal and the error feedback. The converter block diagram is demonstrated in Figure 6.8 [59]. $G_{vd}(S)$ and $G_m(S)$ are the transfer functions of the power conversion and PWM control module, respectively. $H(S)$ is that of the output sampling and $G_c(S)$ is that of the compensating control. The dotted line frame in Figure 6.8 is the external chaotic module. Then, on the basis of analyzing the stability under the normal PWM control, the influence of the external chaotic signal is considered.

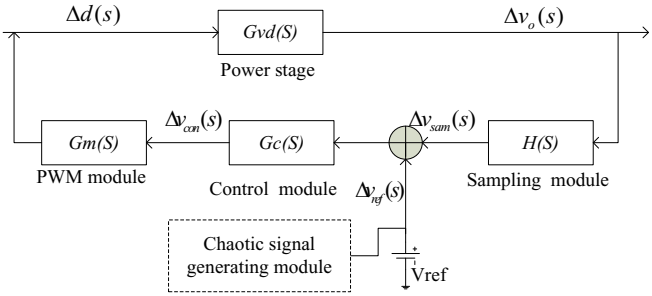


Figure 6.8: System block diagram under chaotic modulation

a. Transfer Function of the Power Conversion

From Figure 6.7, there exists

$$\Delta v_o = \frac{\frac{\mathrm{D}\Delta v_i}{n} + \frac{\Delta d \mathrm{V_i}}{n}}{j\omega L_{eq} + R_{eq} + \left(\frac{1}{j\omega C} + R_{cesr}\right)//R_{load}} \left(\left(\frac{1}{j\omega C} + R_{cesr}\right)//R_{load}\right). \tag{6.35}$$

Conduct the Laplace transformation to equation (6.35),

$$\Delta v_o(S) = \frac{\frac{\mathrm{D}\Delta v_i(S)}{n} + \frac{\Delta d(S) V_i}{n}}{SL_{eq} + R_{eq} + \frac{(1+SCR_{cesr})R_{load}}{SC(R_{cesr}+R_L)}} \frac{(1+SCR_{cesr})R_L}{SC(R_{cesr}+R_L)}. \tag{6.36}$$

So, the transfer function of the output to duty is

$$\begin{aligned} & G_{vd}(S) = \frac{\Delta v_o(S)}{\Delta d(S)} | \Delta v_i(s) = 0 \\ = & \frac{R_L \mathrm{V_i}}{n} \cdot \frac{1 + SR_{cesr}C}{S^2(R_L + R_{cesr})L_{eq}C + S(L_{eq} + CR_{eq}R_L + CR_{eq}R_{cesr} + CR_{cesr}R_L) + R_{eq} + R_L} \\ = & \frac{R_L \mathrm{V_i}}{n(R_{eq} + R_L)} \cdot \frac{1 + \frac{S}{\omega_{z1}}}{1 + 2\xi\left(\frac{S}{\omega_0}\right) + \left(\frac{S}{\omega_0}\right)^2}, \end{aligned} \tag{6.37}$$

where $\omega_0 = \sqrt{\frac{R_{eq}+R_L}{(R_L+R_{cesr})L_{eq}C}}$, $\omega_{z1} = \frac{1}{R_{cesr}C}$, $\xi = \frac{L_{eq}+CR_{eq}R_L+CR_{eq}R_{cesr}+CR_{cesr}R_L}{2\sqrt{(R_{eq}+R_L)(R_L+R_{cesr})L_{eq}C}}$.

From equation (6.37), $G_{vd}(S)$ possesses bi-pole and single zero point, that is

$$\omega_{z1} = \frac{1}{R_{cesr}C}, \omega_{p1} = \omega_0(\xi - \sqrt{\xi^2 - 1}), \omega_{p2} = \omega_0(\xi + \sqrt{\xi^2 - 1}). \tag{6.38}$$

b. Transfer Function of PWM Control

The control signal v_{con} interacts with the sawtooth $v_{sawtooth}$ to regulate the duty of the pulse within PWM control module. According to Eq. (4.4), the maximum and the minimum of $v_{sawtooth}$ are V_U and V_L, and the sawtooth cycle is T, which rises linearly. From Figure 6.9, the control signal v_{con} intersects the sawtooth at the point with the vertical axis v_p. If $v_p = \mathrm{V_U}$, d=0. If $v_p = \mathrm{V_L}$, $d = 1$. The duty d varies along with v_p in inverse proportional linearity.

$$\frac{\Delta d(t)}{\Delta v_{con}(t)} = \frac{1}{\mathrm{V_L} - \mathrm{V_U}} = k_m, \tag{6.39}$$

where k_m is a constant determined by the sawtooth amplitude, and the equivalent gain of PWM control module. The transfer function $G_m(S)$ is expressed as

$$G_m(S) = \frac{\Delta d(S)}{\Delta v_{con}(S)} = k_m. \tag{6.40}$$

For PWM IC TL494 [60], the sawtooth amplitude is 3.5V, so the equivalent gain is

$$k_m = \frac{1}{\mathrm{V_L} - \mathrm{V_U}} = -\frac{1}{3.5}. \tag{6.41}$$

c. Transfer Function of Output Feedback

For the single-output, the sampling module consists of R_b and R, where R_b connects the output terminal and R acts as the pull-down resistor, hence, the transfer function is

$$H(S) = 1 - \frac{R_b}{R_b + R}. \tag{6.42}$$

d. Transfer Function of Compensating Control

Compensating control module is designed according to zero and pole points in equation (6.38). Denote $G_c(S)$ as the transfer function.

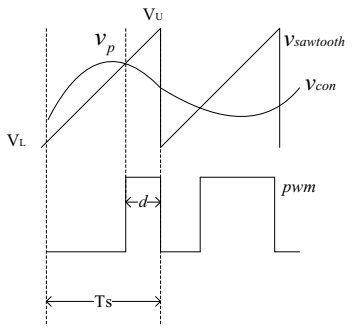


Figure 6.9: Sketch of PWM generation

e. Transfer Function of the Open-Loop System

The stability is estimated by the open-loop amplitude margin and phase margin. The transfer function of the open-loop system is expressed as

$$T(S) = G_c(S)G_m(S)G_{vd}(S)H(S). \tag{6.43}$$

Through taking Eqs. (6.37), (6.41) and (6.42) into Eq. (6.43), the amplitude margin and phase margin of $T(S)$ can be calculated.

f. Effect of Chaotic Modulation on the Stability

Once the external chaotic module connects to the compensating control, the control signal v_{con} becomes chaotic, which makes the duty chaotic. According to the relation between the control signal v_{con} and the sawtooth $v_{sawtooth}$, there are three possibilities during one cycle of the sawtooth, as shown in Figure 6.10.

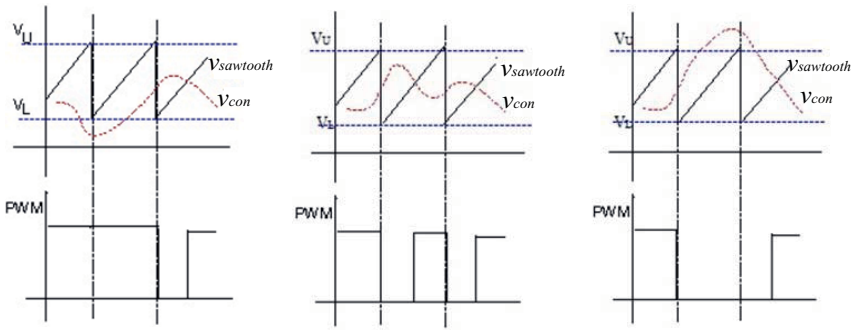
When $v_{con} < v_{sawtooth}$, the pulses of PWM stay at high-level during the whole sawtooth cycle shown as in Figure 6.10 (a).

When v_{con} is greater than the minimum of $v_{sawtooth}$ and less than the maximum of $v_{sawtooth}$, the pulses of PWM retain the variation of high-level and low-level during one cycle, as shown in Figure 6.10 (b).

When $v_{con} > v_{sawtooth}$, the pulses of PWM stay at low-level during the whole sawtooth cycle shown as in Figure 6.10 (c).

Assume that two conditions are satisfied in the converter system. One is to assure PWM in a fixed cycle, during which the switching state goes through "OFF" and "ON" for once. That means that the system performs the switching only once in each cycle T. The other is to assure $\mathrm{V_L} < v_{con} < \mathrm{V_U}$. Under these two preconditions, the transfer function of the chaotic PWM is a constant value k_m, which has no influence on the system stability.

In order to guarantee the stability of the converter with the chaotic duty modulation, the control signal v_{con} is required to meet two conditions accordingly. The first condition is that the frequency (changing speed) of v_{con} is not larger than that of the sawtooth, which allows only one switching motion during one cycle. The second condition is about the



(a) $v_{con} < \mathrm{V_L}$ (b) $\mathrm{V_L} < v_{con} < \mathrm{V_U}$ (c) $v_{con} > \mathrm{V_U}$

Figure 6.10: Three cases of v_{con} and the respective PWM

amplitude of v_{con} which is greater than the minimal of $v_{sawtooth}$ and less than the maximal of $v_{sawtooth}$.
Assume that the system is stable under the normal PWM. From Eq. (4.3), there is

$$v_{con} = \gamma_2 + \gamma_3 v_{ch}. \tag{6.44}$$

Basically, v_{con} is the linearity of the external chaotic signal v_{ch}. The central frequency f_o of v_{ch} represents the evolving speed of v_{con}. The amplitude of v_{con} is determined by γ_2 and γ_3. Because the spectrum of the chaotic signal is mainly distributed in $0 \sim 2f_o$, the conditions that maintain the stability are simplified as
(1) $f_s \geq 2f_o$, that is $f_o \leq \frac{1}{2}f_s$. f_o is the central frequency of the chaotic signal, f_s is the frequency of the sawtooth.
(1) $\mathrm{V_L} < \gamma_2 + \gamma_3 v_{ch} < \mathrm{V_U}$, $\mathrm{V_L}$ and $\mathrm{V_U}$ are the interior parameters of the sawtooth oscillator. The coefficients γ_2 and γ_3 are both determined by the linearity circuit.

6.4 Summary

This chapter applied the circuit average model to study the system stability with the help of the classical control theory. Mainly based on the small signal circuit model of half-bridge topology converter, the system transfer function has been established and the stability analysis has been made. However, the foothold of the chapter was to explore how to keep the system stable under chaotic modulation. Taking the voltage-controlled converter under chaotic modulation as an example, this chapter has drawn a conclusion that the external chaotic signal connecting to PWM module is limited by the amplitude and the central frequency.

7 The Remaining Useful Life under Chaotic Modulation

7.1 Introduction

The service life is a terminology about the prognostic and health management (PHM) [61]. The technology has sprung up in the aerospace and the military fields for decades. The earliest research on PHM technology about electronic products was developed by the Center for Advanced Life Cycle Engineering in University of Maryland. The center put forward the electronic system reliability theory based on physics of failure (PoF). On the basis of PoF, Michael Pecht proposed the concept of the useful life PHM [62, 63], which emphasizes the failure warning, the optimization of maintenance, and the reduction of equipment life cycle cost. Along with the rapid development of PHM, the relative standards have been set, such as IEEE Std-1232 and IEEE P1856.

Prediction technique of the useful life usually refers to predicting the remaining useful life, which belongs to the fault prediction and Health Management. Firstly, based on the characteristics of the product, the key component is figured out for stimulating the failure process. Then, the failure model is built for the key component by focusing on the key parameters. A large amount of data analysis and experimental tests are necessary for the prediction technique. The basic prediction algorithm includes the physical failure model and the statistics analysis.

The switching power supply has already been broadly used in the electronic and electrical system due to its miniaturization and high-efficiency. However, the switching power device has a more potential disability because it works at a higher frequency than the linear power. Besides, it will deteriorate or fail because of over-stress, temperature, moist and over-current. Working status of the power device directly affect the precision, stability and reliability of the system. Its failure and deterioration do harm to the electronic or electrical system [64, 65].

Orsagh and etg al. probed the physical failure models of the electrolytic capacitor and the switch transistor and formed the relation between the component failure and the key parameters in 2005 [65], in which two conclusions have been drawn that the capacitance and the equivalent parallel resistor (ESR) are the critical parameters of the electrolytic capacitor, and the conducting resistance is that of the switch transistor. Li.F.Wu and his team testified that the capacitance falling and ESR rising result in the increase of the output voltage ripples in buck DC converter with computer simulation in 2011[66].

This chapter studies the service life or remaining useful life of a power supply under the chaotic modulation. At present there is a lack of analysis for the effect of chaotic modulation on the remaining useful life of switching converters. Firstly, from the failure modes of the switching converter, the critical components and their failure model are obtained, which lead to the whole converter failing and affect the remaining useful life. Secondly, the research is made for whether or not the chaotic modulation influences the critical compo-

nents. Lastly, chaotic modulation failure is investigated for its impact on the remaining useful life.

7.2 Failure Model of Critical Components

The failure of the switching converter possesses many modes, which are different in creating consequence, emerging probability and the degree of harm. Many literatures about the reliability of the switching power [65, 67, 67–70] report that most of the failures of the power device result from a few components, which is listed in Table 7.1 [65].
Failure modes are related to the circuit topology, component model, variable parameter and operating condition. However, according to the statistical data, the critical components include the electrolytic capacitor, transistor, inductor and rectifying diode whose disability [67, 70] is up to 60%, 31%, 6% and 3% respectively. So, the electrolytic capacitor and the transistor are the focus of the power failure.

a. Electrolytic Capacitor

The output capacitor of the power device acts to filter the high-frequency noise, which suffers from the voltage ripples. The capacitor commonly applies the tantalum capacitor or the aluminum electrolytic capacitor. The tantalum capacitor is characterized by small size, high reliability and high cost, while the aluminum electrolytic capacitor is by high-capacity, low cost and great bulk. Normally, the aluminum electrolytic capacitor is used in the switching power. The main parameters of the capacitor include the capacity, the equivalent serial resistor ESR, current ripple and temperature rise [66]. The equivalent model of the aluminum electrolytic capacitor is shown in Figure 7.1.

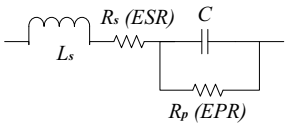


Figure 7.1: The equivalent model of the electrolytic capacitor

For a practical capacitor, its model consists of the capacitor C, the equivalent parallel resistor EPR, the equivalent serial resistor ESR and the inductor L_s. C is the ideal capacitor across the cathode and the anode of the electrolytic capacitor. EPR represents the dielectric loss and the leakage resistance between the cathode and the anode. ESR and L_s are the serial resistance, the equivalent inductance of the electrodes and their connecting points, respectively.
The capacitor failure probably occurs at open-circuit, short-circuit, the capacity decrease and ESR increase, as shown in Table 7.2 [71].

Table 7.1: Failure modes of the switching power

failure mode	component	failure reason	possible effect	occurrence probability	criticality
contact migration	BJT diode	electrical overstress, temperature, high current density	efficiency decrease, conducting resistance increase	high	disastrous
corrosion	BJT diode capacitor MOSFET	moisture	interior corrosion, pad corrosion	low	critical
electrical breakdown	capacitor	electricalal overstress, overvoltage, temperature	short-circuit, open-circuit	high	disastrous
electro migration	BJT diode capacitor MOSFET	electrical overstress, temperature, high current density	metal internal connection failure	low	critical
gate oxide breakdown	MOSFET	electrical overstress, temperature	threshold voltage increase, conducting resistance increase, effeciency decrease	high	disastrous
hot carrier effect	MOSFET	large electrical field in the channel region	short-circuit	low	critical
thermal runaway	BJT diode MOSFET	work-temperature increase, gate oxide breakdown	short-circuit	high	disastrous
thermal cycling	BJT diode capacitor MOSFET	ambient temperature cycle, power fluctuation cycle	thermal runaway	midium high	critical

Table 7.2: Failure mechanism of the aluminum electrolytic capacitor

failure mode	failure behaviour	reason	manufacturing process defects
open-circuit	the connection of the wire and the aluminum foil badly corroded	the conductor influenced by an irregular external stress, use of adhesives and coating agents	bad riveting wire and aluminum foil mechanical stress
short-circuit	the destruction of the oxide film insulation and the electrolytic paper	the conductor influenced by an irregular external stress high temperature, over-use, and over-voltage	metal particle attachment, aluminum foil and wire failure
capacitance decrease	electrolyte volatile, the decrease of the capacitance of anode and cathode foil	over-voltage, great ripple current, charging and discharging frequently, high temperature, and over-use	insufficient electrolyte
ESR increase	internal temperature rise	over-voltage, great ripple current, charging and discharging frequently, high temperature, and over-use	

b. Transistor Switch

There are three kinds of transistors used as the power switch in the switching power, namely, bipolar junction transistor (BJT), metallic oxide semiconductor field effect transistor (MOSFET) and insulated gate bipolar transistor (IGBT). Each possesses its specific failure mode and probability [65]. BJT is of small size and high efficiency, but it works at a low frequency. Oppositely, both of MOSFET and IGBT can work at a high frequency without the priority of the volume and efficiency. MOSFET and IGBT are commonly applied in the switching power because of their high working frequency. Take MOSFET as the example to probe the equivalent circuit model [72], as shown in Figure 7.2. Ron is the resistor between the drain and the source while MOSFET stays "ON". Cgs, Cgd and Cds are the capacitors between the gate and the source, the gate and the drain, the drain and the source, respectively. Lps is the inductor parallelled with the source, which reflects the influence of the distribution parameter. D is the interior diode.

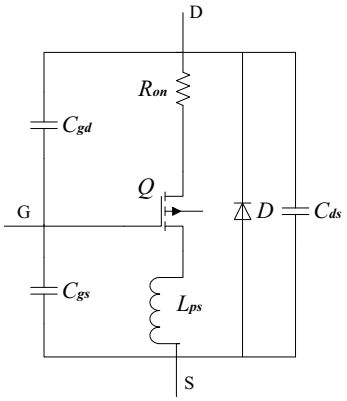


Figure 7.2: The equivalent model of MOSFET

Thermal stress and the electric over-stress result in the increase of Ron, which eventually makes MOSFET degrade or fail. The carriers migrate difficultly under the thermal stress. Less migration or movement leads to the increase of the conducting resistor. As a result, the switching characteristic of the semiconductor changes and MOSFET gradually degrades.

7.3 Impact of Chaotic Modulation on Critical Components

7.3.1 Electrolytic Capacitor

Under chaotic modulation, DC-DC converter is proved to suppress EMI, but its output voltage ripples are increased. The ripples are related with the performance of the elec-

trolytic capacitor, which put forward higher requirements for the capacitor parameters. The electric charge energy is expressed as

$$w = \frac{1}{2}Cv^2, \tag{7.1}$$

where C is the capacitance, v is the voltage across the capacitor and w represents the energy produced by the capacitor.

Denote f_R as the ripple fluctuating frequency of the output voltage in DC-DC converter and P_o as the output power. Within a fluctuation cycle, the capacitor is charged to the maximum v_{p+}, then is discharged to the minimum v_{p-}. Hence, the ripple is described as $v_{pp} = v_{p+} - v_{p-}$. On the basis of Eq. (7.1), there exists

$$P_o \frac{1}{f_R} = \frac{1}{2}C\left(v_{p+}^2 - v_{p-}^2\right), \tag{7.2}$$

and

$$C = \frac{2P_o}{\left(v_{p+}^2 - v_{p-}^2\right) f_R} = \frac{2P_o}{v_{pp}(v_{p+} + v_{p-}) f_R}. \tag{7.3}$$

From Eq. (7.3), the ripple is inversely related to the capacitance. Once the converter generates the slightly larger ripple, the larger-capacity capacitor is required to filter the ripple. The smaller the capacitance, the larger the ripple voltage.

If the ripple voltage is beyond the standard, the capacitor undergoes the excessive ripple current, which leads to the increase of the interior temperature and ESR likewise. Further, the ripple voltage aggravates to be worse. Simultaneously, electrolyte liquid vaporizes with the leakage through the sealing part of the capacitor while the interior temperature rises. Hence, the interior electrolyte liquid is gradually decreased and the capacitance declines. Furthermore, the ripple current brings more heat because of the decrease of the electrolyte liquid. The whole process exacerbates degrading the capacitor, which is shown in Figure 7.3.

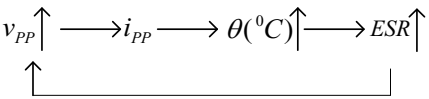


Figure 7.3: Degradation and failure process of capacitor

7.3.2 Power Switch

The power switch mainly refers to the power transistor and the rectifier diode. The switching frequency is regarded as their important parameter. For chaotic duty modulation, the

duty of the transistor driving-pulse chaotically fluctuates based on the nominal duty, but the switching frequency is fixed, which facilitates the switch component selection without the extra requirement. For chaotic frequency modulation, the switching frequency varies in chaos, so the switch is demanded to work at the frequency with the larger margin, which is harsh to select the power switch and design the circuit.

7.4 Failure Influence of Chaotic Modulation

For the chaotic frequency modulation system, the modulation signal changes into the periodic signal if chaotic modulation fails. Compared with the standard PWM control, EMI is reduced under the periodic modulation. But comparing under chaotic modulation and random modulation, the periodic modulation is less effective for EMI reduction [28]. The followings focus on the chaotic duty modulation.

7.4.1 Parameters of Analogue Signal Generator

Take Chua's circuit as the example of chaotic analogue signal generator, as shown in Figure 3.3. One of the key components is the resistor R. The resistance of R varies due to the thermal stress and humidity. With the inductor L as 18 mH, when $R = 1600\ \Omega$, the circuit runs in chaos. The voltage trajectory between C_1 and C_2 is tested under the different resistance of R by adjusting R within the 25% variation. Figure 7.4 shows the simulations with the software PROTUES, where the circuit appears some different status like the single-period, multi-period, single-scroll and bi-scroll once the resistor varies.
When the modulation signal extracted from Chua's circuit changes from chaos to period, chaotic modulation fails.

7.4.2 Operation Precision of Digital Signal Generator

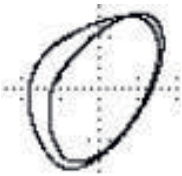
A chaotic digital signal generator is commonly realized by MCU or MPU, which is limited by the arithmetic precision. Hence, some information is lost while MCU or MPU is processing the float-point calculation. The higher the arithmetic precision is, the less information it loses. The chaotic digital signal derivers from the discrete maps through the iteration. No matter how high the arithmetic precision is, iterative process eventually enable the variable to go from the chaos to the period, as shown in Figure 7.5. Chapter 4 has presented the solution for keeping chaos.

7.4.3 Simulations

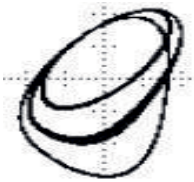
For the chaotic duty modulation, the EMI suppression would be less effective if chaotic modulation turns into the period modulation. The modulated duty is expressed as

$$d(t) = \mathrm{D} + \Delta d, \tag{7.4}$$

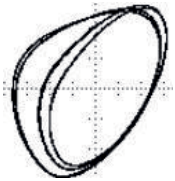
where D is the duty under the normal PWM control and Δd is the duty offset while modulating. From Eq. (7.4), there are the following conclusions.



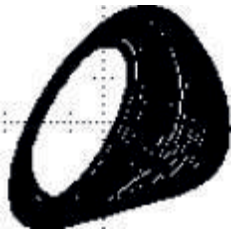
(a) 2-period $R = 1990\ \Omega$



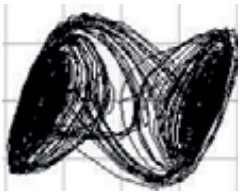
(b) 3-period $R = 1820\ \Omega$



(c) 4-period $R = 1885\ \Omega$

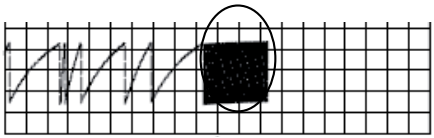


(d) Single-scroll $R = 1800\ \Omega$

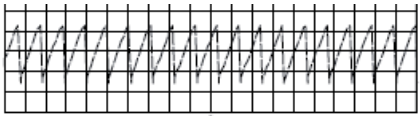


(e) Bi-scroll $R = 1600\ \Omega$

Figure 7.4: Trajectory of $v_2 - v_1$ with various R in Chua's circuit



(a) Evolving waveform (s/Div: 500 ms)



(b) Fractionated gain (s/Div:2.47 ms)

Figure 7.5: From chaos to periodic status

when Δd is equal to zero, modulation pulse possesses the fixed duty D.
When Δd is chaotic, modulation pulse is consequently chaotic.
When Δd is periodic, modulation pulse is also periodic.
If the modulation signal connected to PWM module changes from the chaos to the periodic state, Δd is likewise. Chaotic modulation turns into the period modulation, From Chapter 1, period modulation scatters the energy of the fundamental f_c and its harmonics nf_c into $[nf_c \cdot (1 - \frac{\alpha}{2}), nf_c \cdot (1 + \frac{\alpha}{2})], n \geq 1$ with the interval of f_s (α is the modulation coefficient and f_s is the periodic frequency). Period modulation reduces the EMI energy at the fundamental component and its harmonics, but the spread spectrum is less effective when compared that under chaotic modulation.
Based on Figure 2.5, the schematic is made for simulation, where the external chaotic signal produced by Chua's circuit is injected to the PWM control module of the buck converter. Figures 7.6 and 7.7 demonstrate the evolving waves from the chaos state to the period state by simulating Chua's circuit.
Under chaotic modulation, v_{ch}, PWM, i_L and their FFTs are shown in Figure 7.6 from top to bottom. Under the period modulation, v_{ch}, PWM, i_L and their FFTs are shown in Figure 7.7.

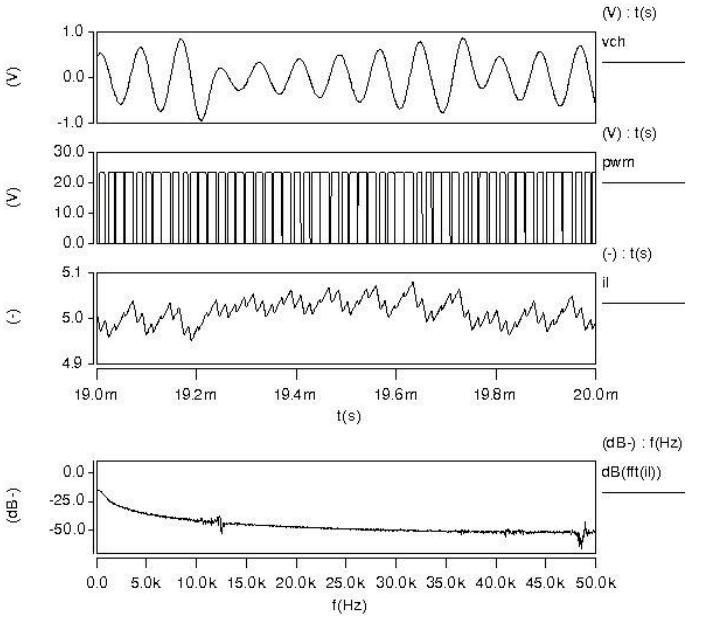


Figure 7.6: FFT of v_{ch}, PWM, i_L and i_L under chaos modulation

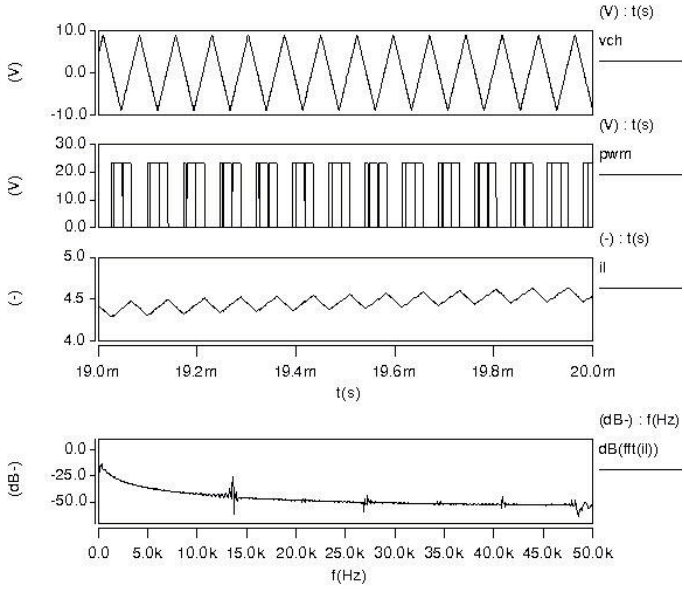


Figure 7.7: FFT of v_{ch}PWMi_L and i_L in periods

The comparisons illustrate that once Chua's circuit evolves from chaos to period, the following happens.
a. The amplitude of the signal v_{ch} increases.
b. PWM probably happens to lose some pulses.
c. i_L changes into the periodic wave.
d. The FFTs appear the larger peak that means EMI suppression reduced.
e. From the chaos state to the period state, an extra frequency is fixed to the converter and a risk of resonance oscillation is added to some components in the converter , such as the capacitor, the transformer and the conductor.

7.5 Summary

This chapter made the research for the remaining useful life of the switching converter on the viewpoint of the fault prediction and Health Management. According to the statistics, the critical components of the switching converter are the electrolytic capacitor and the transistor switch.
ESR is the key parameter of the electrolytic capacitor. Chaotic modulation normally leads to the increase of the output ripple, making the ESR increase and the capacitance reduce. Therefore, it is obliged to limit the amplitude of the output voltage ripple while designing and applying the converter under chaotic modulation. Otherwise, over-ripple makes the capacitor degrade and fail, which shortens the useful life of the whole switch

power supply. The chaotic duty modulation keeps the cycle unchanged, so the modulation has no impacts on the power switches. However, chaotic frequency modulation makes the switching frequency change within a range, so the modulation influences the power switches and demands the switches with an enough margin of the working frequency. Meanwhile, the possible failure of chaotic modulation will influence the service life of the switching converter. A chaotic analogue signal generator, such as Chua's circuit, fails to output the chaotic signal because of variable parameters under high temperature and humidity. The chaotic digital signal generator varies from chaos to periods due to the limited float precision of MCU or MPU. Once chaotic modulation fails, the modulation mode becomes a periodic modulation, weakening the EMI reduction.

8 Tests of Input and Output Characteristics

8.1 Introduction

Some researchers have reported the experimental tests about the effects of the chaotic modulation on efficiency, power factor, current harmonics and output ripples [17, 21, 22]. In addition to these items, commercial power devices are obliged to confront a series of prescribed tests like the reliability, functional specifications, protection features, safety regulations and other specific requirements.
Functional specifications mainly refer to voltage regulation, load regulation, output ripple and noise, power factor, efficiency, energy efficiency ratio, rise time, fall time, boot delay time, holdup time, overshoot amplitude and output transient response. Protection features include over-voltage protection, short-circuit protection and over-current protection. Safety regulations involve the input current, leakage current, voltage insulation, temperature resistance, chassis ground, transformer output characteristic and negative tests. There are some other specific tests , such as electrostatic discharge, fast transient or impulse interference, surge, voltage drop or interruption and boot impulse current.
For a switching converter, protection functions through some sensors and actuators, where these sensors separately detect over-voltage, short-circuit and over-current, and the correspondent actuator responds executing. Although the protection module acts on PWM control, it is independent of the latter. Hence, chaotic modulation will not affect the protection features. Meanwhile, safety regulations emphasize the safe clearance, ground, flame retardancy of components, transformer output characteristic and abnormal operation, which don't involve PWM control. Therefore, protection features and safety regulations are neglected while analyzing the effect of chaotic modulation on system performance. Chaotic modulation is essentially the closed loop control of output feedback, which influences the input and output of the system. From the stability analysis in Chapter 5, chaotic modulation has no impact on the system stability, as long as the chaotic signal meets the requirements of amplitude and central frequency in chaotic duty modulation. Chapter 6 probes the effects of chaotic modulation on the useful life of the system from the aspects of health management technology, failure modes and critical components of the switching converter. Consequently, the output ripple resulting from chaotic modulation should be confined. By combining the converter function with other specific requirements of the switching converter, this chapter focuses on the testing specification of the input and output characters.

8.2 Input Characteristics

Switching converters normally make use of single-phase two-wire power as the input. The AC specification depends on the country or the region that uses the grid, which is catego-

rized as 90 V ∼ 132 V (rated value as 115 V) and 180 V ∼ 264 V (rated value as 230 V), both with the working frequency range of 47 Hz ∼ 63 Hz. The input characteristics cover efficiency, power factor, voltage drop interrupt and inrush current. Voltage drop interrupt refers the state that the electrical equipment can not be damaged when the input voltage drops or breaks instantly. Inrush is about the current spikes that occur when the device switches on or off frequently. Voltage drop interrupt and inrush current are both for examining whether the power device can protect itself or not.
As for the efficiency and power factor, the test conditions about the input voltage and the output loads are uniform. The input voltage is normally specified as 115 V/60 Hz, 230 V/50 Hz or 220 V/50 Hz/60 Hz depending on the area of the customer. The output load is commonly considered as three levels of the maximum load, its fifth and its half. The input power p_{in} and output power p_{out} are separately measured under different loads. The input current i_{in} can be tested when p_{in} refers to the active power. Based on the above, the efficiency and the power factor (PF) can be calculated.

8.3 Output Characteristics

The Output characters are demanded that the output voltage and current meet the rated requirements under the rated loads. Besides, the precision and the transient response of output should be considered when the input voltage or the output load varies. The voltage precision refers to the voltage regulation ratio, load regulation ratio and the ripple and noise of output. Denote u_o as the output voltage, u_{max} as the maximum, u_{min} as the minimum and u_{rate} as the rated output.

8.3.1 Voltage Accuracy

a. Voltage Regulation Ratio
Voltage regulation ratio means the stability of the output voltage varying along with AC input voltage at a certain load, which is required less than 1%. The test process is
(1) Keeping the load at a fixed value
(2) Keeping the working frequency at a certain value from 47 Hz to 63 Hz
(3) Regulating the input voltage from 90 V to 132 V (rated value $u_{rate} = 115$ V) or from 180 V to 264 V (rated value $u_{rate} = 230$ V) and noting the maximum u_{max} and minimum u_{min} of output voltage
(4) Applying the mathematical formula $(u_{max} - u_{min})/u_{rate} \cdot 100\%$ to calculate the voltage regulation ratio
b. Load Regulation Ratio
Load regulation ratio refers to the stability of the output voltage varying along with the load at a certain AC input voltage, which is required less than ±5%. The test process is
(1) Keeping the AC input voltage at a fixed value within 90 V ∼ 132 V or 180 V ∼ 264 V
(2) Keeping the working frequency at a certain value from 47 Hz to 63 Hz
(3) Regulating the load and noting the maximum u_{max} and minimum u_{min}
(4) Applying the mathematical formula $(u_{max} - u_{rate})/u_{rate} \cdot 100\%$ or $(u_{min} - u_{rate})/u_{rate} \cdot 100\%$ to calculate the Load regulation ratio

Table 8.1: Test conditions

Frequency (Hz)	Max Load (W)	50% Load (W)	20% Load (W)
50	200	100	40

Table 8.2: Efficiency at maxLoad

Item	p_{in} (W)	i_{in} (A)	p_{out}(W)	$Effi$ (%)	$\cos\alpha$ (%)
Normal PWM	264.6	1.64	200	75.6	70.0
chaotic PWM	266.3	1.67	200	75.1	69.5

8.3.2 Output Transient Response

Output transient response means the stability of output voltage varying along with the rapidly changing output load, which is specified that the maximum and the minimum of the output voltage aren't greater than $\pm 10\%$ of u_{rate}.

8.4 Comparisons of Test Results

By taking PC's power as the test bed, tests are conducted under the normal PWM and the chaotic PWM, respectively. The rated full-load power of this device is 200 W, whose test conditions are listed in Table 8.1.

Tables 8.2, 8.3 and 8.4 list the efficiency when AC input is 230 V and the working frequency is 50 Hz. In the tables p_{in}, i_{in} and p_o are the test results. The efficiency is calculated as $Effi = p_{out}/p_{in} \cdot 100\%$, and the power factor is $\cos\alpha = p_{in}/(230 i_{in}) \cdot 100\%$.

Tables 8.5 and 8.6 list the efficiency and the power factor at the different load, where three different loads are considered. The total efficiency is the efficiency average at three loads and the total power factor is likewise. From the tables, the efficiency and power factor under chaotic modulation are slightly lower than those under the normal PWM, because the external chaotic signal generator is powered by the test object, PC's power device, which increases the system load.

Tables 8.7 and 8.8 list the voltage regulation ratios of +12V output and +5V output. While regulating the input voltage from 180 V to 250 V (u_{rate}=230 V), the output voltage varies and the maximum u_{max} and the minimum u_{min} are produced. The voltage regulation ratio is calculated by the expression $(u_{max} - u_{min})/u_{rate} \cdot 100\%$. Although the voltage regulation ratios are slightly greater under chaotic modulation than the normal modulation, they are still less than the limit of 1%.

Tables 8.9 and 8.10 are load regulation ratio of two outputs, +12 V output and +5V

Table 8.3: Efficiency at 1/2 Load

Item	p_{in} (W)	i_{in} (A)	p_{out}(W)	$Effi$ (%)	$\cos\alpha$ (%)
Normal PWM	126.9	0.81	100	78.8	68.0
chaotic PWM	128.0	0.83	100	78.1	67.5

Table 8.4: Efficiency at 1/5 Load

Item	p_{in} (W)	i_{in} (A)	p_{out} (W)	$Effi$ (%)	$\cos\alpha$ (%)
Normal PWM	52.7	0.36	40	75.9	63.5
chaotic PWM	52.8	0.37	40	75.7	62.7

Table 8.5: Efficiency (%)

Item	MaxLoad	50% Load	20% Load	Average
Normal PWM	75.6	78.8	75.9	76.8
chaotic PWM	75.4	78.1	75.7	76.4

Table 8.6: Power factor (%)

Item	MaxLoad	50% Load	20% Load	Average
Normal PWM	70.0	68.0	63.5	67.2
chaotic PWM	69.5	67.5	62.7	66.6

Table 8.7: Voltage regulation ratio of +12V output

Item	u_{max}(V)	u_{min}(V)	Voltage regulation ratio (%)
Normal PWM	12.06	12.01	0.41
chaotic PWM	12.05	11.95	0.83

Table 8.8: Voltage regulation ratio of +5 V output

Item	u_{max}(V)	u_{min}(V)	Voltage regulation ratio(%)
Normal PWM	5.02	4.98	0.8
chaotic PWM	5.035	4.99	0.9

Table 8.9: Load regulation ratio of +12V output

Item	Max Load	50%Load	20%Load	0%Load	Load reg-ratio 1	Load reg-ratio 2
Normal PWM	11.6V	11.8V	11.85V	12.5V	4.2	-3.3
chaotic PWM	11.65V	11.85V	11.87V	12.5V	4.2	-3.0

Table 8.10: Load regulation ratio of +5 V output

Item	Max Load	50%Load	20%Load	0%Load	Load reg-ratio 1	Load reg-ratio 2
Normal PWM	4.85V	4.90V	4.95V	5.05V	1.0	-3.0
chaotic PWM	4.88V	4.95V	5.0V	5.08V	1.6	-2.4

output. Keeping the input voltage at 230 V and the working frequency at 50 Hz, the tests proceed under the load at Max Load, 50% Load, 20% Load and no-load, respectively. According to the expressions $(u_{max} - u_{rate})/u_{rate} \cdot 100\%$ and $(u_{min} - u_{rate})/u_{rate} \cdot 100\%$, the load regulation ratios are achieved. Comparisons show that chaotic modulation affect the load regulation ratio in accordance with the normal PWM control.
Table 8.11 list the output ripple and noise. The tests are conducted under same conditions as the previous one. The respective output ripple is obtained and recorded at Max Load, 50% Load, 20% Load and no-load. The test results indicate that chaotic PWM results in increasing the ripple within the limit of specification.

8.5 Summary

Regarded as the research object, a PC's power supply has been tested under normal PWM control and chaotic PWM control, respectively. It shows that the efficiency and PF are slightly lower under chaotic PWM control than the normal one by comparison. The regulation ratio of voltage and load almost keep steady under this two controls. Besides, the output ripples are slightly greater under the chaotic PWM control than the normal one. However, all the test results are within the scope permitted by the respective specifications. In a word, the chaotic modulation schedule applied in this project is proved to be feasible.

Table 8.11: Tests of output ripples

Item	Max Load	50% Load	20% Load	0% Load
Normal PWM (+12 V output)	96 mV	86 mV	74 mV	20 mV
chaotic PWM (+12 V output)	102 mV	98 mV	81.8 mV	50 mV
Normal PWM (+5 V output)	40 mV	36 mV	30 mV	18 mV
chaotic PWM (+5 V output)	48 mV	40 mV	38 mV	30 mV

9 Conclusions

Switching converters play an important role in many fields. However, converters produce serious electromagnetic interference (EMI) because of high change rates of current and voltage by applying PWM technology to control switching actions of transistors. Therefore, it is obliged to suppress EMI for application of switching converters. Chaotic modulation has been developed to suppress EMI of the switching converter by dispersing the energy into a wide frequency band and smoothing the peaks of the EMI spectrum. Chaotic frequency modulation is most commonly reported for EMI suppression in switching converters, which features the varying working frequency and thus increases the difficulty in designing circuitry parameters. Hence, this research aims at the chaotic duty modulation and probes into its feasibility and practicability. The main contributions are summarized as following.

a. The chaotic duty modulation has been concerned in this dissertation, instead of the well studied chaotic frequency modulation. Chaotic duty modulation is just to change the duty of the transistor driving-pulse while maintains the fixed switching frequency, which facilitates the hardware design of switching converters. Chaotic duty modulation has been realized by appending an external chaotic signal to the existing PWM module of the switching converter, which is practicable without the loss of the generality.

b. The central frequency of a chaotic signal has been verified to affect the EMI suppression. With the help of the central frequency, the effectiveness of EMI suppression is studied on relating to chaotic signals used for chaotic modulation. The central frequency is defined as the frequency corresponding to the largest spectral peak of a chaotic signal, which is an attribute of chaotic system decided by interior parameters. Quantitative analysis, simulation and experimental results have verified that it will reach the optimal EMI suppression under chaotic duty modulation when the central frequency of chaotic signal is close to a half of the switching frequency, providing a reference for engineering application.

c. A qualitative verification has been conducted for the stability of switching converters under chaotic modulation via the classic control theory. Based on the half-bridge model, stability can be judged by the margin of the gain and the phase in the way of the normal control transfer function, which requires that the external chaotic signal connecting to PWM module is limited by the amplitude and the central frequency. The two preconditions can be described: 1) the chaotic signal switches in every period T synchronously for only once; 2) the control voltage meets the condition $V_L < v_{con} < V_U$.

d. Through the failure model and critical components, the remaining useful life is also ensured under chaotic duty modulation. As for typical input and output characteristics testing items, comparisons have been made between normal PWM and chaotic modulation. The testing results indicate that the efficiency of the switching converter under chaotic modulation is slightly lower than that under the normal PWM, and voltage regulation ratio, load regulation ratio and output ripples are slightly higher, but all within the permitted scope. Therefore, it is verified that this proposal of using the chaotic duty modulation in

switching converters for EMI suppression is feasible in practice and lays a foundation for industrial applications.

In addition, some tasks will be further done in the future as follows:

a. The research on frequency character of chaotic signal is confined to the specific analogue and chaos mapping, so exploration in-depth will be given for the general chaotic signal. The relation between the output ripples and the central frequency will be strictly deduced.

b. The stability analysis is confined to the chaotic duty modulation, more modulation modes will be investigated and compared to find out a universal way of the stability analysis. Meanwhile, it is useful to research how to apply the non-linear kinetic modeling.

c. The further research is about the impacts chaotic modulation on the magnetic components, such as the transformer and inductor. It is significant to study the magnet and the heat under chaos in order to provide some theory bases for the EMC design.

References

[1] L. Bert and P. Robert. Power converters and voltage regulators. *Omnidirectional Inductive Powering for Biomedical Implants Analog Circuits and Signal Processing*, pages 83–117, 2009.

[2] A. Pressman. *Switching power supply design*. McGraw-Hill, Inc., 1997.

[3] B. Vtezslav, G. John, and A. Duncan. *Power semiconductor devices: theory and applications* . Wiley, 1999.

[4] S. Banerjee and G. Verghese. *Nonlinear phenomena in power electronics: bifurcations, chaos, control, and applications*. Wiley-IEEE Press [Imprint], 2001.

[5] IEC. *IEC 60050*, 1990.

[6] R. Clayton. *Introduction to electromagnetic compatibility*. Wiley, 1992.

[7] R. Bracewell. *The fourier transform and its applications3rd ed.* Boston, McGraw Hill, 2000.

[8] L. Ahlfors. *Complex analysis*. McGraw Hill, 1979.

[9] K. Chen and T. A. Stuart. Soft switch-avalanche igbt convertor. *Electronics Letters*, 26(19):1623–1625, 1990.

[10] P. Caldeira, R. Liu, D. Dalal, and W. Gu. Comparison Of EMI performance of PWM and resonant power converters. *Power electronics specialists conference, 1993. PESC '93 record., 24th annual IEEE*, pages 134 – 140, 1993.

[11] H. Mao, F. C. Lee, X. Zhou, H. Dai, M. Cosan, and D. Boroyevich. Improved zero-current transition converters for high-power applications. *Industry Applications, IEEE Transactions on*, 33(5):1220–1232, 1997.

[12] D.-Y. Lee, M.-K. Lee, D.-S. Hyun, and I. Choy. New zero-current-transition PWM DC/DC converters without current stress. *Power Electronics, IEEE Transactions on*, 18(1):95–104, 2003.

[13] D. Zhang, D. Y. Chen, and F. C. Lee. An experimental comparison of conducted EMI emissions between a zero-voltage transition circuit and a hard switching circuit. In *Power Electronics Specialists Conference, 1996. PESC'96 Record., 27th Annual IEEE*, volume 2, pages 1992–1997. IEEE, 1996.

[14] M. Martins, H. Grundling, H. Pinheiro, J. Pinheiro, and H. Hey. A ZVT PWM boost converter using an auxiliary resonant source. In *Applied powere lectronics conference and exposition, 2002. APEC 2002. seventeenth annual IEEE*, volume 2, pages 1101–1107. IEEE, 2002.

[15] H. Chung, S. Hui, and K. Tse. Reduction of power converter EMI emission using soft-switching technique. *Electromagnetic Compatibility, IEEE Transactions on*, 40(3):282 – 287, 1996.

[16] H. Iu and B. Robert. Control of chaos in a PWM current-mode H-bridge inverter using time-delayed feedback. *Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on*, 50(8):1125 – 1129, 2003.

[17] H. Li, K. S. W. TANG, Z. Li, and W. A. Halang. A chaotic peak current-mode boost converter for EMI reduction and ripple suppression. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2008.

[18] R. Yang and B. Zhang. Chaotification control of buck converter via time-delayed feedback. *Acta Physica Sinica*, 56(7), 2007.

[19] Y. Zhou, C. Tse, and S. Qiu. Applying resonant parametric perturbation to control chaos in the Buck dc/dc converter with phase shift and frequency mismatch considerations. *International Journal of Bifurcation and Chaos*, 13(11):3459–3471, 2003.

[20] J. Gao and J. Xiong. Research into the reduction of electromagnetic interference level of Boost DC/DC converter by chaotic modulation signals with different sources. *Journal of FuJian University of Technology*, 2004.

[21] R. Yang and Z. Bo. Experiment and mechanism research of chaotic PWM of converter in EMI suppressing. *Proceedings of the CSEE*, 27(10):114–119, 2007.

[22] H. Li, Z. Li, B. Zhang, F. Wang, N. Tan, and W. Halang. Design of analogue chaotic PWM for EMI suppression. *Electromagnetic Compatibility, IEEE Transactions on*, 52(4):1001–1007, 2010.

[23] H. Li, Z. Li, F. Lin, and B. Zhang. Suppressing harmonics in four-quadrant AC-DC converters with chaotic SPWM control. *International Journal of Circuit Theory and Applications*, 42:331–342, 2014.

[24] K. Tse, H.-H. Chung, S. R. Hui, and H. So. A comparative investigation on the use of random modulation schemes for DC/DC converters. *Industrial Electronics, IEEE Transactions on*, 47(2):253–263, 2000.

[25] K. Tse, H. Chung, S. Hui, and H. So. Analysis and spectral characteristics of a spread-spectrum technique for conducted EMI suppression. *Power Electronics, IEEE Transactions on*, 15(2):399–410, 2000.

[26] A. M. Stankovic, G. C. Verghese, and D. J. Perreault. Analysis and synthesis of randomized modulation schemes for power converters. *Power Electronics, IEEE Transactions on*, 10(6):680–693, 1995.

[27] D. Stone, B. Chambers, and D. Howe. Random carrier frequency modulation of PWM waveforms to ease EMC problems in switched mode power supplies. In *Power Electronics and Drive Systems, 1995., Proceedings of 1995 International Conference on*, pages 16–21. IEEE, 1995.

[28] K. Tse, H. Chung, S. Hui, and H. So. A comparative study of carrier-frequency modulation techniques for conducted EMI suppression in PWM converters. *Industrial Electronics, IEEE Transactions on*, 49(3):618–627, 2002.

[29] W. Zhou and S. Qiu. EMI suppression technology for switching power supply. *Low Voltage Apparatus*, 19, 2008.

[30] K. Tse, R. Ng, H. Chung, and S. Hui. An evaluation of the spectral characteristics of switching converters with chaotic carrier-frequency modulation. *Industrial Electronics, IEEE Transactions on*, 50(1):171–182, 2003.

[31] S. Callegari, R. Rovatti, and G. Setti. Spectral properties of chaos-based FM signals: theory and simulation results. *Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on*, 50(1):3–15, 2003.

[32] N. X. Quyen, V. Van Yem, and T. M. Hoang. Chaotic modulation based on the combination of CPPM and CPWM. In *Nonlinear Dynamics and Synchronization (INDS) & 16th Int'l Symposium on Theoretical Electrical Engineering (ISTET), 2011 Joint 3rd Int'l Workshop on*, pages 1–6. IEEE, 2011.

[33] R. Yang and B. Zhang. Quantification description of the chaotic PWM spectrum of the switching converter. *Acta Physica Sinica*, 55(11):5667–5673, 2006.

[34] M. Balestra, M. Lazzarini, G. Setti, and R. Rovatti. Experimental performance evaluation of a low-EMI chaos-based current-programmed DC/DC boost converter. In *Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on*, pages 1489–1492. IEEE, 2005.

[35] A. Amini and J. Nazarzadeh. Improvement behavior and chaos control of buck converter in current mode controlled. In *IEEE Int. Conference on Industrial Technology*, pages 1–6. IEEE, 2008.

[36] H. Li, Z. Li, B. Zhang, W. K. Tang, and W. Halang. Suppressing electromagnetic interference in direct current converters. *Circuits and Systems Magazine, IEEE*, 9(4):10–28, 2009.

[37] P. Aruna and L. Premalatha. Investigation of EMI reduction in buck converter by using external chaos generator. In *Recent Advancements in Electrical, Electronics*

and Control Engineering (ICONRAEeCE), 2011 International Conference on, pages 520–525. IEEE, 2011.

[38] Y. Song, Z. Li, J. Niu, G. Zhang, W. Halang, and H. Hirsch. Reducing EMI in a PC power supply with chaos control. In *Foundations and Applications of Intelligent Systems*, pages 231–241. Springer, 2014.

[39] W. Zhou and S. Qiu. Effect of chaotic spectrum-spread on output voltage ripple of power converter. *Electric Power Automation Equipment*, 28(12):52–55, 2008.

[40] A. V. Oppenheim, A. Willsky, and S. Nawab. Signals and systems 2nd ed, 1997.

[41] L. Ruan and K. Chen. Chua's circuit chaotic signal spectrum distribution characteristics and its application in the circuit design. *Journal of circuits and systems*, 3(1):8–13, 1998.

[42] L. Jackson, A. Lindgren, Y. Kim, *et al.* A chaotic attractor from Chuas circuit. *IEEE Transactions on Circuits and Systems*, 31(12), 1984.

[43] B. Liu. *Nonlinear dynamics and chaos*. Northeast normal university press, 1994.

[44] M. P. Kennedy. Three steps to chaos. II. a Chua's circuit primer. *Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on*, 40(10):657–674, 1993.

[45] A. S. Elwakil and M. P. Kennedy. Improved implementation of Chua's chaotic oscillator using current feedback op amp. *Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on*, 47(1):76–79, 2000.

[46] G. Jiang and Y. Cheng. Study on Chua's nonlinear chaotic circuit and its frequency characteristic. *Journal of EEE*, 24:5–7, 2002.

[47] Y. Song, Z. Li, J. Niu, G. Zhang, W. Halang, and H. Hirsch. Reducing EMI in multiple-output DC converters with chaos control. In *World Scientific Proc. Series on Computer Engineering and Information Science 7; Uncertainty Modeling in Knowledge Engineering and Decision Making - Proceedings of the 10th International FLINS Conf.*, pages 1155–1160, 2012.

[48] Motorola. *Switch mode pulse width modulation control circuit*.

[49] A. Elwakil and M. Kennedy. Chua's circuit decomposition: a systematic design approach for chaotic oscillators. *Journal of the Franklin Institute*, 337(2):251–265, 2000.

[50] I. Takuya, K. Keiji, K. Hideki, and H. Kentaro. An experimental suppression of spatial instability in one-way open coupled chua's circuits. *International Journal of Bifurcation and Chaos*, 12(12):2897–2905, 2002.

[51] R. D. Middlebrook and S. Cuk. A general unified approach to modelling switching-converter power stages. *In: Power Electronics Specialists Conference*, 42(6):18–34, 1976.

[52] D. Czarkowski and M. Kazimierczuk. A new and systematic method of modeling PWM DC-DC converters. In *Systems Engineering, 1992., IEEE International Conference on*, pages 628–631, 1992.

[53] H. Li, Z. Li, B. Zhang, Q. Zheng, and W. Halang. The stability of a chaotic PWM boost converter. *International Journal of Circuit Theory and Applications*, 39(5):451–460, 2011.

[54] J. Xu, v. Caliskan, and C. Lee. Transient time-domain analysis of zero-current switching quasi-resonant converters. *Applied Power Electronics Conference and Exposition-APEC94Conference Proceedings,Ninth Annual*, pages 1028–1034, 1994.

[55] D. Czarkowski and M. Kazimierczuk. Circuit models of PWM half-bridge DC-DC converter. In *Circuits and Systems, 1992., Proceedings of the 35th Midwest Symposium on*, pages 469–472. IEEE, 1992.

[56] A. K. Bhat and S. Dewan. Analysis and design of a high-frequency resonant converter using LCC-type commutation. *Power Electronics, IEEE Transactions on*, (4):291–301, 1987.

[57] G. Qiu and X. Luo. *Circuitry*. Higher Education Press, 5 edition, 2011.

[58] C. Ouyang and Y. Yan. A new method for modeling PWM DC-DC converters. *Journal of Nanjing University of Aeronautics and Astronautics*, 33(3):254–258, 2001.

[59] M. Lee, J. Lio, D. Y. Chen, Y. Chen, and Y. Wu. Small-signal modeling of multiple-output flyback converters in continuous conduction mode with weighted feedback. *IEEE Transactions on Industrial Electronics*, 45(2):236–248, 1998.

[60] Intel Corporation. *ATX12V power supply design guide*, version 2.2 edition, 2005.

[61] Y. Zhou, J. Bo, and T. Wei. A review of current prognostics and health management system related standards. *Chemical Engineering*, 33, 2013.

[62] M. Pecht. *Prognostics and health management of electronics*. Wiley Online Library, 2008.

[63] M. Pecht and J. Gu. Physics-of-failure-based prognostics for electronic products. *Transactions of the Institute of Measurement and Control*, 31(3-4):309–322, 2009.

[64] R. Callan and B. Larder. The development and demonstration of a probabilistic diagnostic and prognostic system (ProDAPS) for gas turbines. In *Aerospace Conference Proceedings, 2002. IEEE*, volume 6, pages 6–3083. IEEE, 2002.

[65] R. Orsagh, D. Brown, M. Roemer, T. Dabnev, and A. Hess. Prognostic health management for avionics system power supplies. In *Aerospace Conference, 2005 IEEE*, pages 3585–3591. IEEE, 2005.

[66] W. Lifeng, Z. S. Du Yinyu, G. Yong, and P. Wei. Effect of electrolytic capacitors on the life of SMPS. *Journal of Convergence Information Technology*, 6(6):491–499, 2011.

[67] A. Lahyani, P. Venet, G. Grellet, and P. Viverge. Failure prediction of electrolytic capacitors during operation of a switchmode power supply. *Power Electronics, IEEE Transactions on*, 13(6):1199–1207, 1998.

[68] H. Zhang, R. Kang, M. Luo, and M. Pecht. Precursor parameter identification for power supply prognostics and health management. In *Reliability, Maintainability and Safety, 2009. ICRMS 2009. 8th International Conference on*, pages 883–887. IEEE, 2009.

[69] X. Shao and X. Li. A new approach of determining critical components in electronic systems based on the theory of PoF. In *Computational Intelligence and Design (ISCID), 2011 Fourth International Symposium on*, volume 2, pages 266–270. IEEE, 2011.

[70] USA: Department of Defense. *Military handbook-reliability prediction of electronic equipment*, mil-hdbk-217f edition, 1995.

[71] K. Abdennadher, P. Venet, G. Rojat, J.-M. Retif, and C. Rosset. A real-time predictive-maintenance system of aluminum electrolytic capacitors used in uninterrupted power supplies. *Industry Applications, IEEE Transactions on*, 46(4):1644–1652, 2010.

[72] X. Zheng, L. Wu, Y. Guan, and X. Li. Analysis of the degradation of MOSFETs in switching mode power supply by characterizing source oscillator signals. *Mathematical Problems in Engineering*, 2013, 2013.

Curriculum Vitae

Affiliation and Official Address: Faculty of Mathematics and Computer Science FernUniversität in Hagen, 58084 Hagen, Germany
Date and Place of Birth:01 December 1970, Hubei, P.R.China **Gender:** Female

Languages: Chinese(native language), English

Education:
Ph.D. in Electrical Engineering, Faculty of Mathematics and Computer Science, FernUniversität in Hagen, Germany, 2011-2016
M.Sc. in Circuitry and System, School of Electronics and Information Engineering, South China University Technology, 2001-2004
B.Sc. in Agricultural Electrification and AutomationInstitute of Agricultural Engineering Shenyang Agricultural University, 1990-1994

Specialisation:
(1) Main Fields: Embedded System and Their Applications in Appliances
(2) Present: Suppression of Electromagnetic Interference in Power Supplies

Online-Buchshop für Ingenieure

VDI nachrichten

BUCHSHOP

Online-Shops

Fachliteratur und mehr - jetzt bequem online recherchieren & bestellen unter: www.vdi-nachrichten.com/Der-Shop-im-Ueberblick

Täglich aktualisiert: Neuerscheinungen VDI-Schriftenreihen

Im Buchshop von vdi-nachrichten.com finden Ingenieure und Techniker ein speziell auf sie zugeschnittenes, umfassendes Literaturangebot.

Mit der komfortablen Schnellsuche werden Sie in den VDI-Schriftenreihen und im Verzeichnis lieferbarer Bücher unter 1.000.000 Titeln garantiert fündig.

Im Buchshop stehen für Sie bereit:

VDI-Berichte und die Reihe **Kunststofftechnik**:

Berichte nationaler und internationaler technischer Fachtagungen der VDI-Fachgliederungen

Fortschritt-Berichte VDI:

Dissertationen, Habilitationen und Forschungsberichte aus sämtlichen ingenieurwissenschaftlichen Fachrichtungen

Newsletter „Neuerscheinungen":

Kostenfreie Infos zu aktuellen Titeln der VDI-Schriftenreihen bequem per E-Mail

Autoren-Service:

Umfassende Betreuung bei der Veröffentlichung Ihrer Arbeit in der Reihe Fortschritt-Berichte VDI

Buch- und Medien-Service:

Beschaffung aller am Markt verfügbaren Zeitschriften, Zeitungen, Fortsetzungsreihen, Handbücher, Technische Regelwerke, elektronische Medien und vieles mehr – einzeln oder im Abo und mit weltweitem Lieferservice

Die Reihen der Fortschritt-Berichte VDI:

1 Konstruktionstechnik/Maschinenelemente
2 Fertigungstechnik
3 Verfahrenstechnik
4 Bauingenieurwesen
5 Grund- und Werkstoffe/Kunststoffe
6 Energietechnik
7 Strömungstechnik
8 Mess-, Steuerungs- und Regelungstechnik
9 Elektronik/Mikro- und Nanotechnik
10 Informatik/Kommunikation
11 Schwingungstechnik
12 Verkehrstechnik/Fahrzeugtechnik
13 Fördertechnik/Logistik
14 Landtechnik/Lebensmitteltechnik
15 Umwelttechnik
16 Technik und Wirtschaft
17 Biotechnik/Medizintechnik
18 Mechanik/Bruchmechanik
19 Wärmetechnik/Kältetechnik
20 Rechnerunterstützte Verfahren (CAD, CAM, CAE CAQ, CIM ...)
21 Elektrotechnik
22 Mensch-Maschine-Systeme
23 Technische Gebäudeausrüstung

ISBN 978-3-18-385010-5